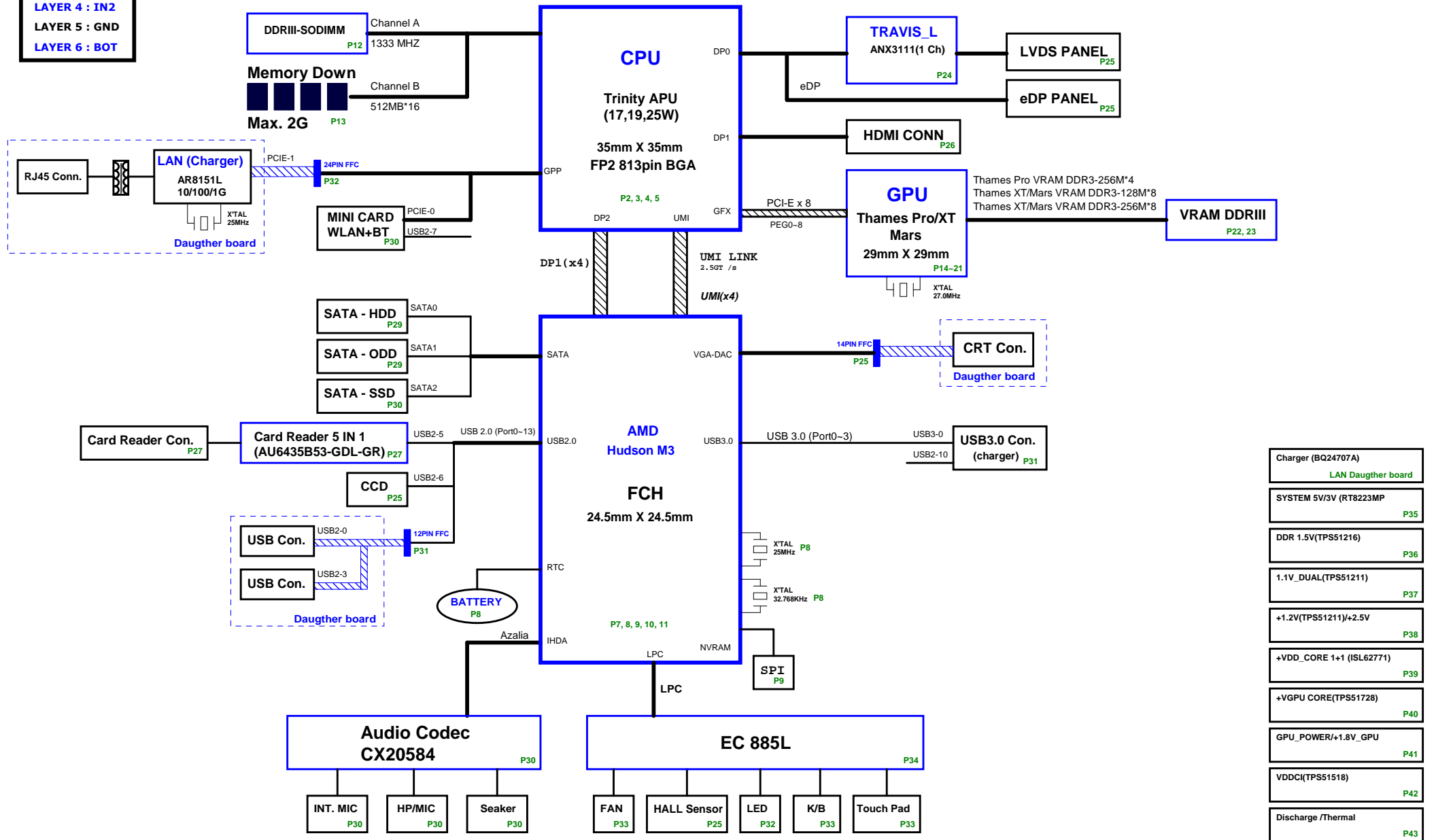


## PCB STACK UP

LAYER 1 : TOP  
 LAYER 2 : SVCC  
 LAYER 3 : IN1  
 LAYER 4 : IN2  
 LAYER 5 : GND  
 LAYER 6 : BOT

## 15.6" ZRP Block Diagram

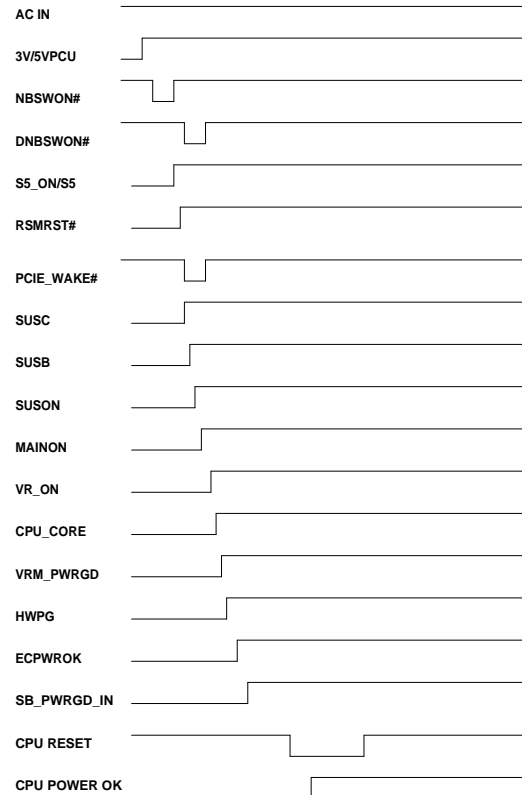


Charger (BQ24707A)	LAN Daughter board
SYSTEM 5V/3V (RT8223MP)	P35
DDR 1.5V(TPS51216)	P36
1.1V_DUAL(TPS51211)	P37
+1.2V(TPS51211)/+2.5V	P38
+VDD_CORE 1+1 (ISL62771)	P39
+VGPU CORE(TPS51728)	P40
GPU_POWER/+1.8V_GPU	P41
VDDCI(TPS51518)	P42
Discharge /Thermal	P43

## BOM Option

ITEM	DESCRIPTION	MARK
1	LVDS Panel Sku	LVDS@
2	eDP Panel Sku	eDP@
3	VGA Sku	EV@
4	VGA Thames Sku	EV_T@
5	VGA Mars Sku	EV_M@
6	VGA Sku for Thames and Mars stuff different value parts	EV_SP@
7	GPU 128bit Sku	EV_128@
8	GPU 128bit Sku of Special part value change	EV_128SP@
9	USB Charge Functions Sku	CH@
10	No USB Charge Functions Sku	NCH@
11	USB3.0 Re-Driver Sku	RD@
12	No USB3.0 Re-Driver Sku	NRD@
13	Always connect functions Sku	AC@
14	No Always connect functions Sku	NAC@
15	Special part value change or modify for different BOM sku	SP@

## Power Sequence



## Hudson M3 SM BUS

FCH SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD26 AD25	DDR / RFID
SCLK1 SDATA1 (+3V_S5)	T7 R7	not used
SCLK2 SDATA2 (+3V_S5)	H19 G19	EC
SCLK3 SDATA3 (+3VPCU)	G22 G21	BATTERY
SCL4 SDATA4 (+3V_S5)	J19 K19	not used

## KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

EC	FCH	Device I2C_Device(S)			
I2Ce_1(M)	I2Cf_2(M)	Charger	Battery		ALL/S5
I2Ce_2(M)		APU			ALL
I2Ce_3(M)					
	I2Cf_3(M)	APU			S5
	I2Cf_1(M)				S5
	I2Cf_0(M)	DDR	WLAN/3G	Image Sensor	S0

EC will Conflict with FCH.  
Do not mount

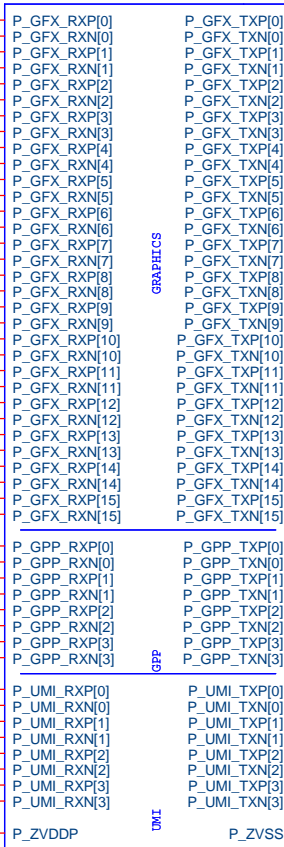
02



**Quanta Computer Inc.**  
**PROJECT : ZRP**

Size	Document Number	Rev
		A1A
SYSTEM INFORMATION		
Date: Tuesday, May 29, 2012	Sheet 2 of 44	

U25A



SP@TRINITY APU\_BGA813

SP : A10(AJ04655UT01)  
 A8(AJ04555VT01)  
 A6(AJ04455UT01)  
 A4(AJ04355UT00)

AN1 PEG\_TXP0\_C  
 AN2 PEG\_TXN0\_C  
 AM4 PEG\_TXP1\_C  
 AM3 PEG\_TXN1\_C  
 AK2 PEG\_TXP2\_C  
 AK1 PEG\_TXN2\_C  
 AH1 PEG\_TXP3\_C  
 AH2 PEG\_TXN3\_C  
 AF3 PEG\_TXP4\_C  
 AF4 PEG\_TXN4\_C  
 AE1 PEG\_TXP5\_C  
 AE2 PEG\_TXN5\_C  
 AD4 PEG\_TXP6\_C  
 AD3 PEG\_TXN6\_C  
 AB2 PEG\_TXP7\_C  
 AB1 PEG\_TXN7\_C

C537 EV@0.1u/10V\_4  
 C540 EV@0.1u/10V\_4  
 C541 EV@0.1u/10V\_4  
 C550 EV@0.1u/10V\_4  
 C555 EV@0.1u/10V\_4  
 C563 EV@0.1u/10V\_4  
 C569 EV@0.1u/10V\_4  
 C575 EV@0.1u/10V\_4

C534 EV@0.1u/10V\_4  
 C538 EV@0.1u/10V\_4  
 C544 EV@0.1u/10V\_4  
 C557 EV@0.1u/10V\_4  
 C561 EV@0.1u/10V\_4  
 C568 EV@0.1u/10V\_4  
 C565 EV@0.1u/10V\_4  
 C572 EV@0.1u/10V\_4

PEG\_TXP0 14  
 PEG\_TXN0 14  
 PEG\_TXP1 14  
 PEG\_TXN1 14  
 PEG\_TXP2 14  
 PEG\_TXN2 14  
 PEG\_TXP3 14  
 PEG\_TXN3 14  
 PEG\_TXP4 14  
 PEG\_TXN4 14  
 PEG\_TXP5 14  
 PEG\_TXN5 14  
 PEG\_TXP6 14  
 PEG\_TXN6 14  
 PEG\_TXP7 14  
 PEG\_TXN7 14

FP2 only support PEG X 8

14 PEG\_RXP0  
 14 PEG\_RXN0  
 14 PEG\_RXP1  
 14 PEG\_RXN1  
 14 PEG\_RXP2  
 14 PEG\_RXN2  
 14 PEG\_RXP3  
 14 PEG\_RXN3  
 14 PEG\_RXP4  
 14 PEG\_RXN4  
 14 PEG\_RXP5  
 14 PEG\_RXN5  
 14 PEG\_RXP6  
 14 PEG\_RXN6  
 14 PEG\_RXP7  
 14 PEG\_RXN7

FP2 only support PEG X 8

TO WLAN  
 TO LAN

28 PCIE\_RXP0\_WLAN  
 28 PCIE\_RXN0\_WLAN  
 32 PCIE\_RXP1\_LAN  
 32 PCIE\_RXN1\_LAN

AG7 PCIE\_TXP0\_C  
 AG8 PCIE\_TXN0\_C  
 AE7 PCIE\_TXP1\_C  
 AE8 PCIE\_TXN1\_C  
 AD7  
 AD8  
 AB6  
 AB5

C45 0.1u/10V\_4  
 C74 0.1u/10V\_4

C53 0.1u/10V\_4  
 C67 0.1u/10V\_4

PCIE\_TXP0\_WLAN 28  
 PCIE\_TXN0\_WLAN 28  
 PCIE\_TXP1\_LAN 32  
 PCIE\_TXN1\_LAN 32

8 UMI\_RXP0  
 8 UMI\_RXN0  
 8 UMI\_RXP1  
 8 UMI\_RXN1  
 8 UMI\_RXP2  
 8 UMI\_RXN2  
 8 UMI\_RXP3  
 8 UMI\_RXN3

AM10 P\_UMI\_RXP[0]  
 AN10 P\_UMI\_RXN[0]  
 AM8 P\_UMI\_RXP[1]  
 AM8 P\_UMI\_RXN[1]  
 AP8 P\_UMI\_RXP[2]  
 AR8 P\_UMI\_RXN[2]  
 AR7 P\_UMI\_RXP[3]  
 AP7 P\_UMI\_RXN[3]

P\_UMI\_TXP[0]  
 P\_UMI\_TXN[0]  
 P\_UMI\_TXP[1]  
 P\_UMI\_TXN[1]  
 P\_UMI\_TXP[2]  
 P\_UMI\_TXN[2]  
 P\_UMI\_TXP[3]  
 P\_UMI\_TXN[3]

AN6 UMI\_TXP0\_C  
 AM6 UMI\_TXN0\_C  
 AP6 UMI\_TXP1\_C  
 AR6 UMI\_TXN1\_C  
 AP4 UMI\_TXP2\_C  
 AR4 UMI\_TXN2\_C  
 AP3 UMI\_TXP3\_C  
 AR3 UMI\_TXN3\_C

C508 0.1u/10V\_4  
 C507 0.1u/10V\_4  
 C511 0.1u/10V\_4  
 C513 0.1u/10V\_4

UMI\_TXP0 8  
 UMI\_TXN0 8  
 UMI\_TXP1 8  
 UMI\_TXN1 8  
 UMI\_TXP2 8  
 UMI\_TXN2 8  
 UMI\_TXP3 8  
 UMI\_TXN3 8

+1.2V\_VDDP R372 196/F\_6 P\_ZVDDP AR11

AP11 P\_ZVSS R371 196/F\_6



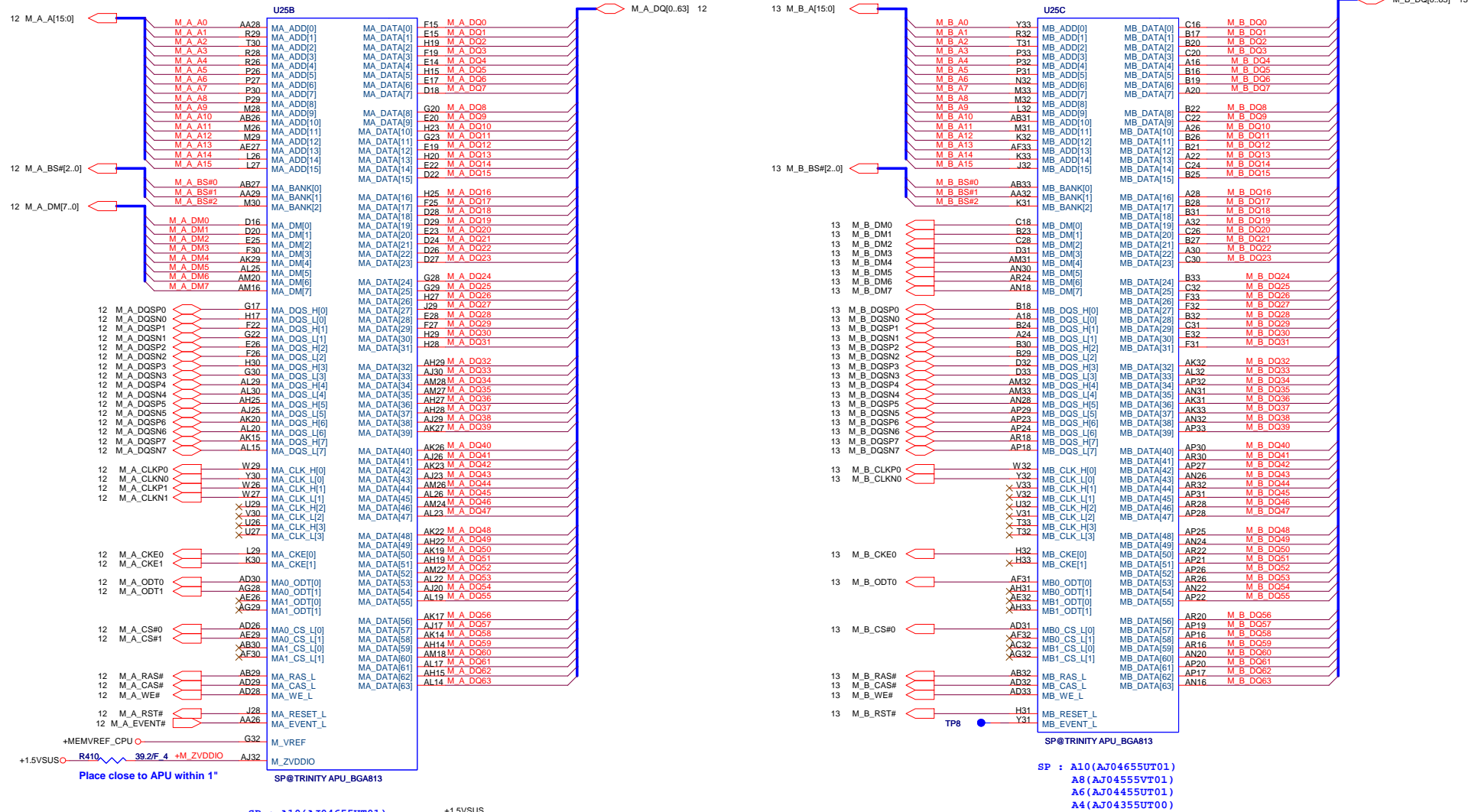
Quanta Computer Inc.

PROJECT : ZRP

Size	Document Number	Rev
	APU 1/4(PCIE/UMI/GPP/HDT)	A1A

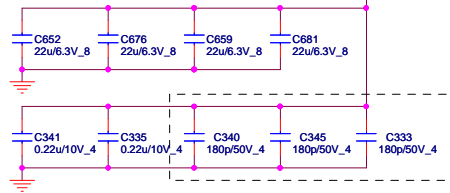
Date: Friday, June 01, 2012 Sheet 3 of 44

## Soldermask openings for all bottom side vias/TPs under FS1

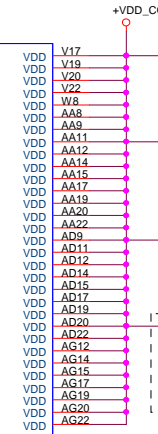
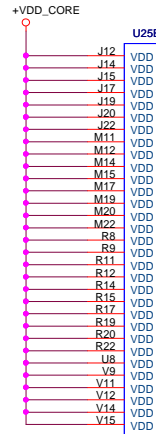




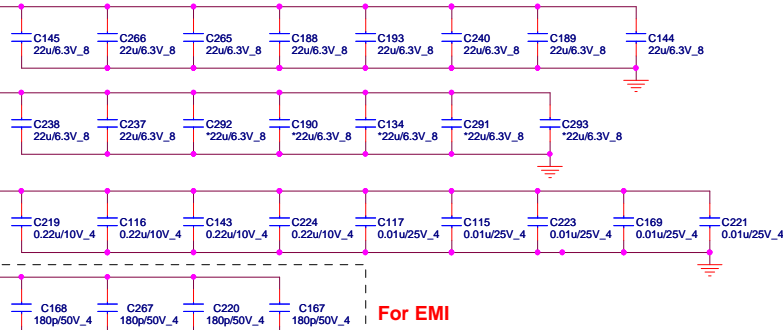
### 22A Maximum IDDNBspike 33A



For EMI



### 22A Maximum IDDspike 35A

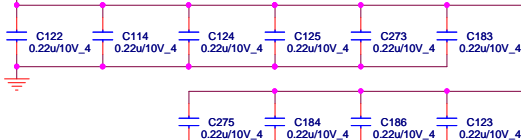


For EMI

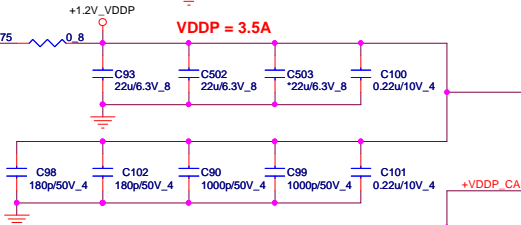
### APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	1.0V ~ 1.3V
VDDNB	+VDDNB_CORE	1.05V ~ 1.325V
VDDIO	+1.5VSUS	1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDA	+2.5V_VDDA	+2.5V

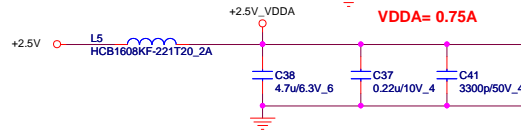
### 2.3A Up to DDR3-1333 @ 1.5V VDDIO



### VDDP = 3.5A



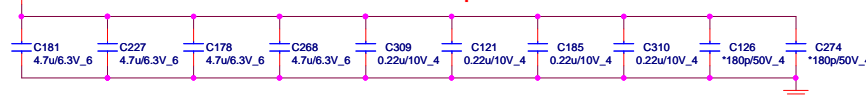
### VDDA = 0.75A



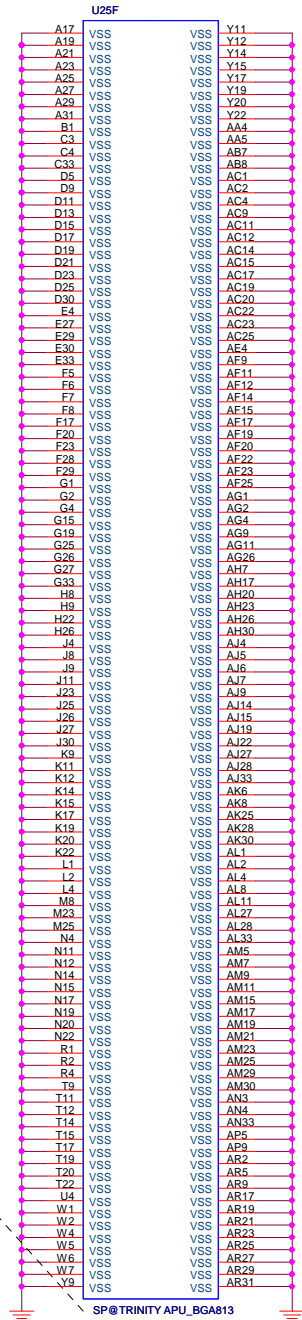
SP : A10(AJ04655UT01)  
A8(AJ04555VT01)  
A6(AJ04455UT01)  
A4(AJ04355UT00)

### DECOUPLING between PROCESSOR and DIMMs

#### Across VDDIO and VSS split



If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

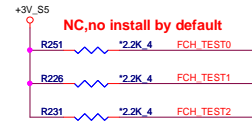


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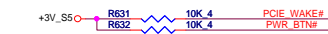
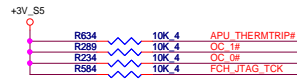
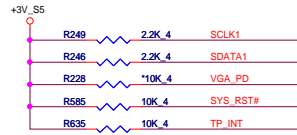
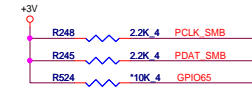
PROJECT : ZRP

APU 4/4(POWER/GND)

Size	Document Number	Rev
		A1A
Date:	Friday, June 01, 2012	Sheet 6 of 44

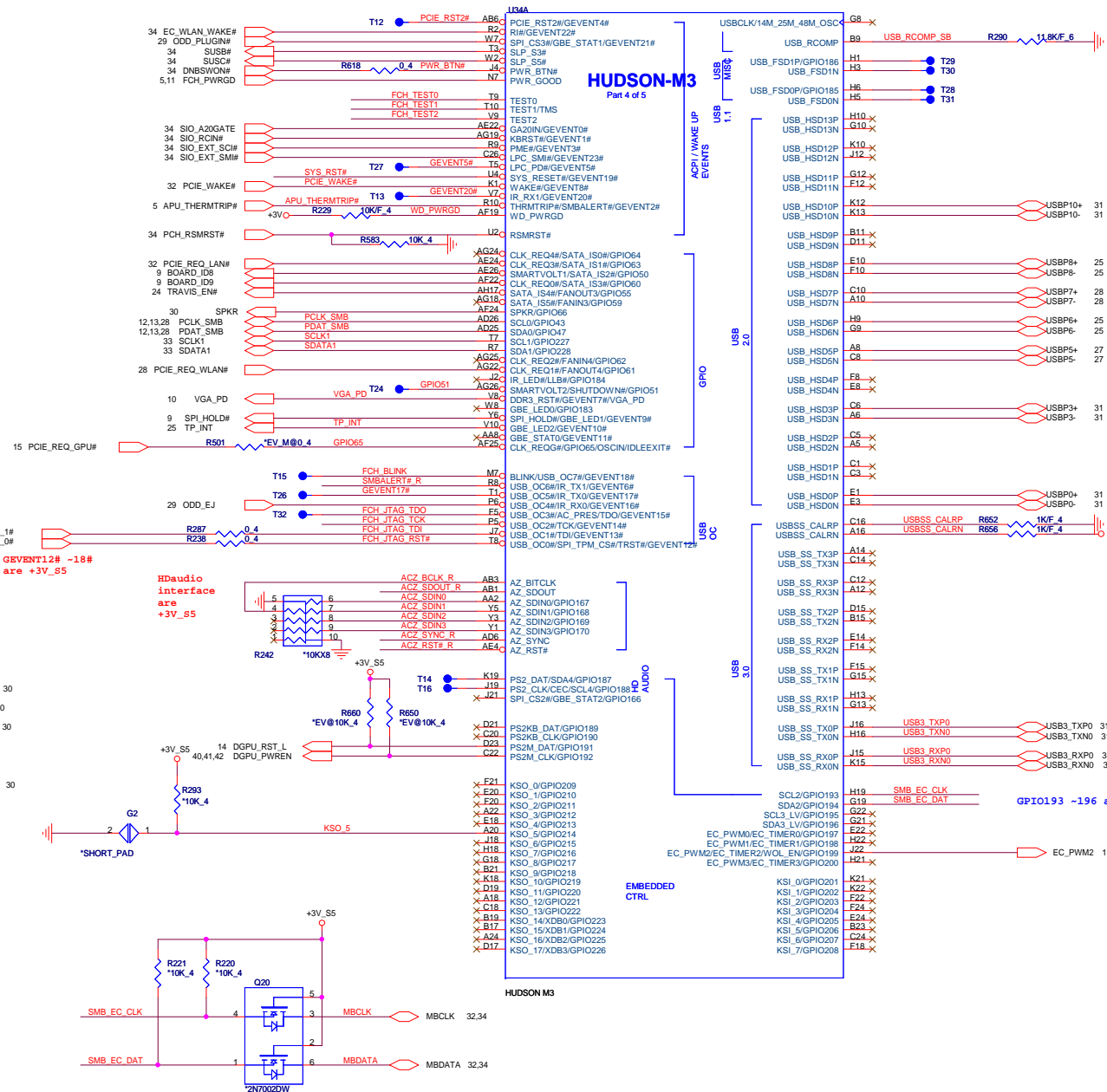
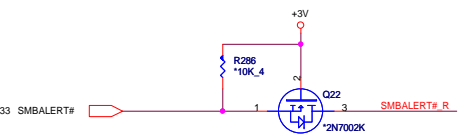
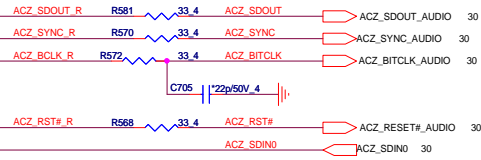


remove pull hi ( chip internal have pull hi )

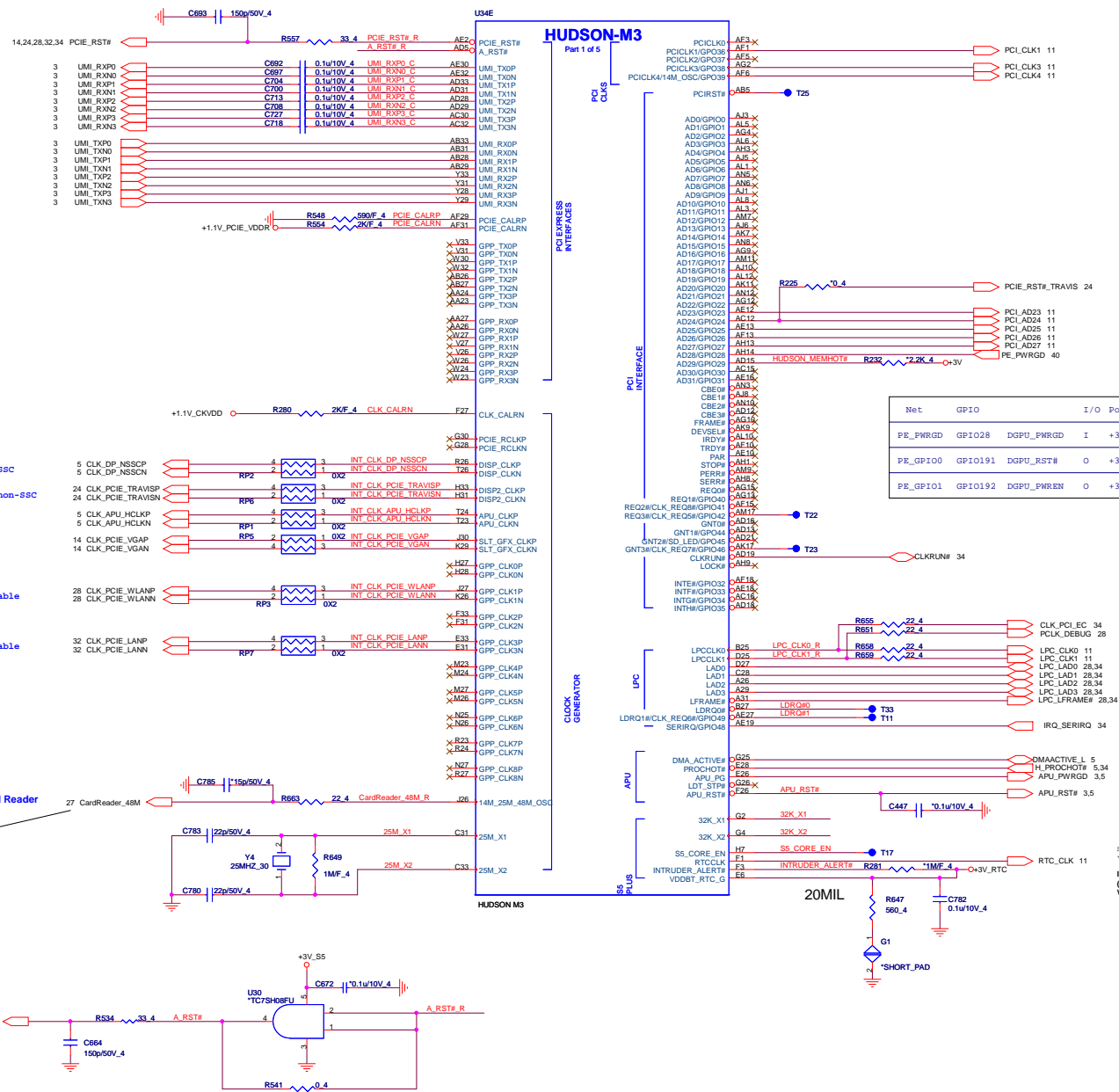


Note:LLB#, WAKE# and PWR\_BTN need pull up +3VPCU only if S5+ mode is supported

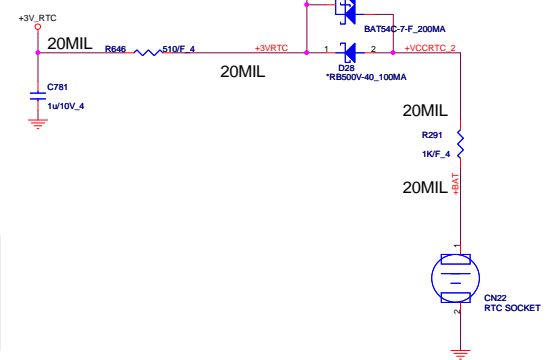
## To Azalia







## RTC Circuitry(RTC)





SATA0 HDD

SATA1 ODD

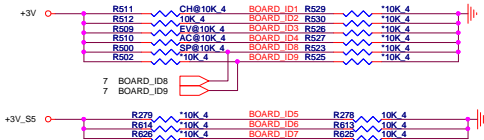
SATA2 SSD



Integrated Clock Mode: SATA\_X1, SATA\_X2 leave unconnected.

SP : stuff R705 for ELPIDA DRAM  
no stuff R705 for HYNIX DRAM

Initial BIOS set internal pull down

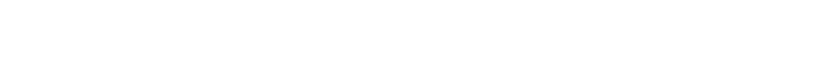
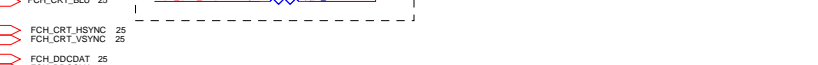
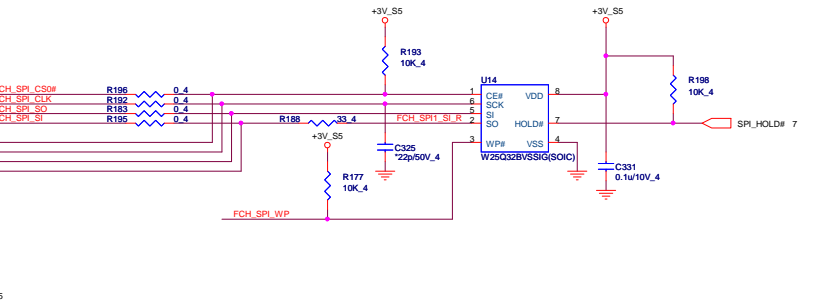
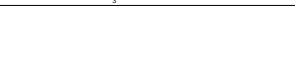
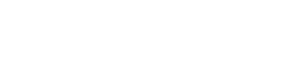
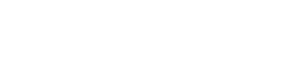
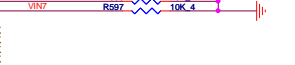
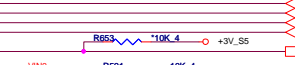
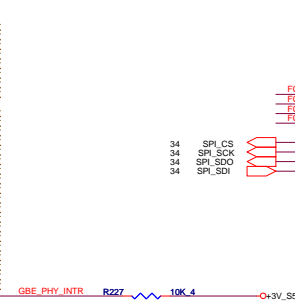
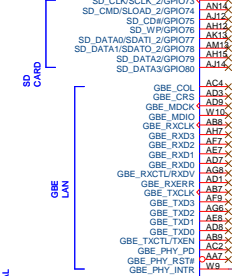


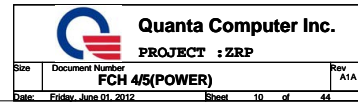
## BOARD ID SETTING ID5, ID6, ID7 S5 Power State

Board ID	ID1	ID2	ID3	ID4	ID5	ID6	ID7	ID8	ID9
USB Charge	H								
No USB Charge	L								
Synaptics ELAN		H							
VGA SKU			H						
UMA SKU				H					
AC				H					
No AC				L					
Reserve					H				
Reserve					L				
Reserve						H			
ELPIDA DRAM							H		
HYNIX DRAM							L		
Reserve								H	

## HUDSON-M3

Part 2 of 5

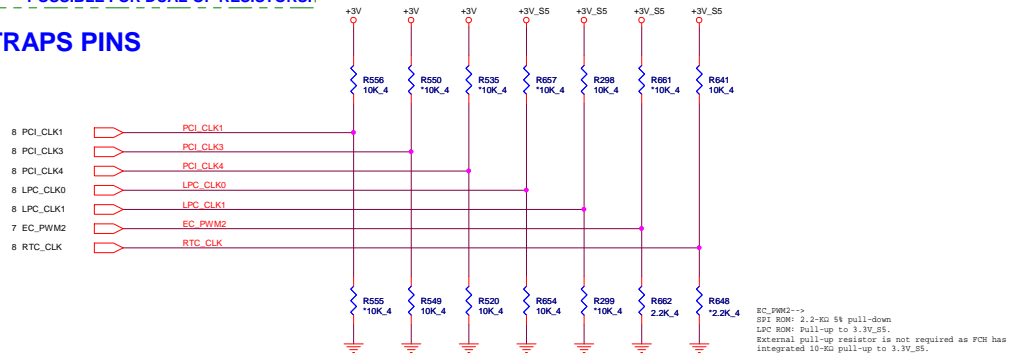






OVERLAP COMMON PADS WHERE  
POSSIBLE FOR DUAL-OP RESISTORS.

## STRAPS PINS



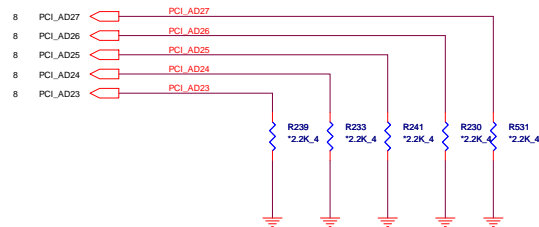
## REQUIRED STRAPS

Remove PCI\_CLK2 function

	-----	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	-----	ALLOW PCIE Gen2 DEFAULT	-----	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	SS PLUS MODE DISABLED DEFAULT
PULL LOW	-----	FORCE PCIE Gen1	-----	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	SPI ROM DEFAULT	SS PLUS MODE ENABLED

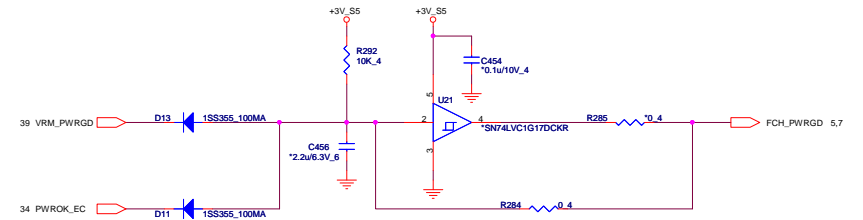
## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

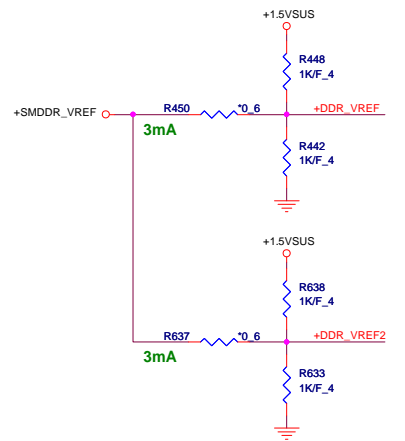
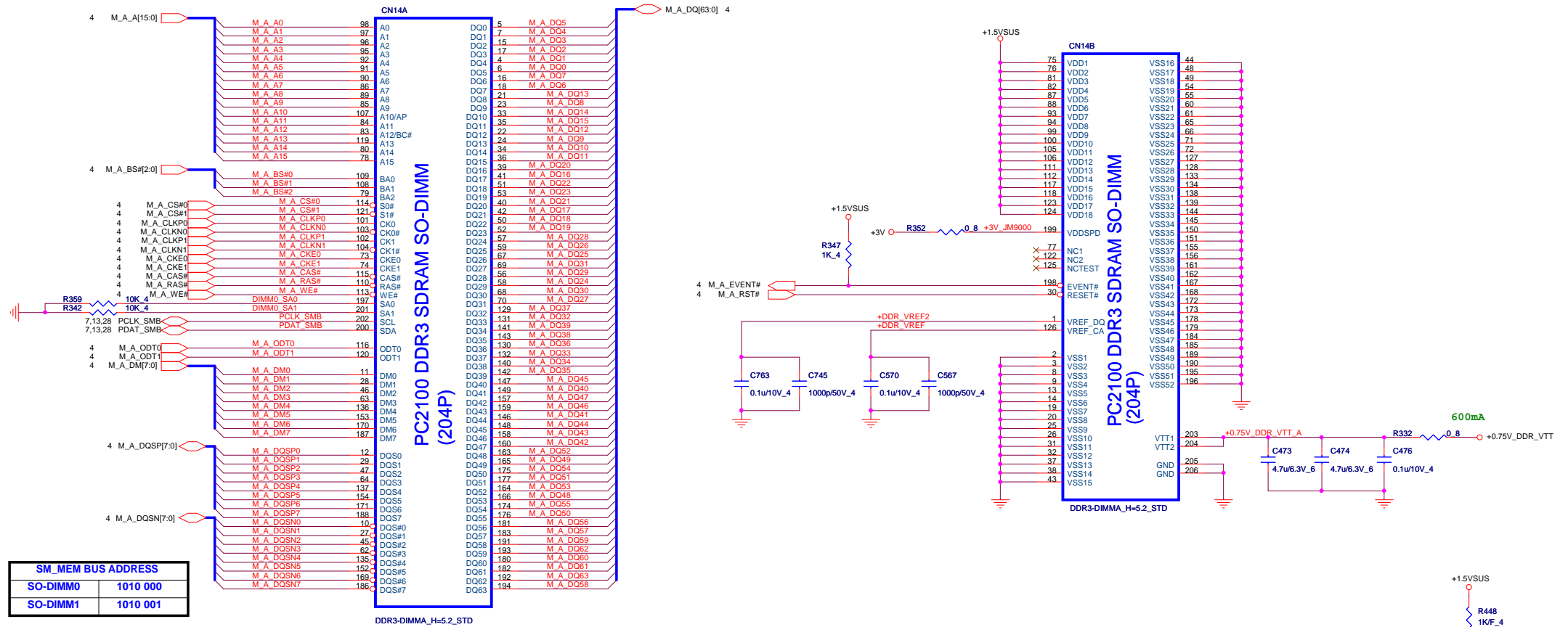


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

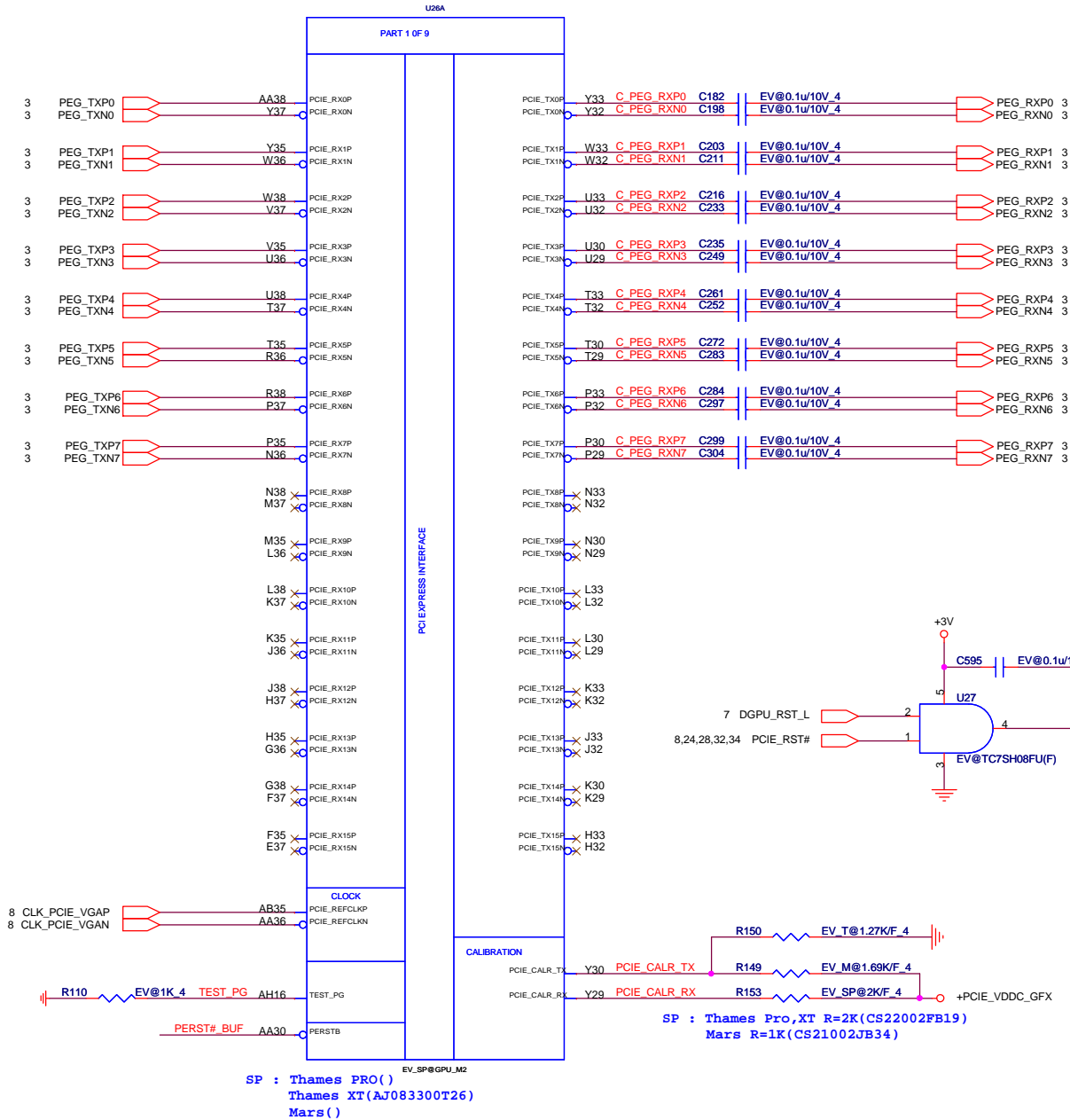
## FCH PWRGD CKT



## DDR3 DIMM-A







## Thames(Pro,XT) and Mars Power-on sequence PX5.0(no BACO)

DGPU\_PWREN

VDDC/VDDCI/1.8V\_IO  
MVDDQ/+PCIE\_VDDC  
VDDR3

20ms max

PE\_PWRGD

PWRGOOD

1.00ms

PCIE\_RST#

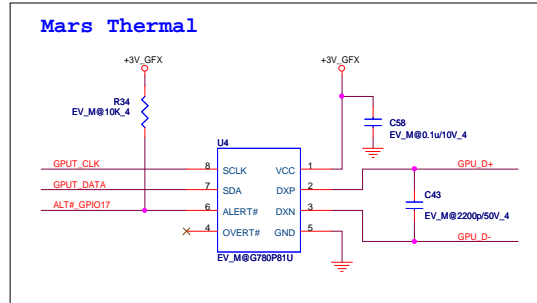
PCIE Clock



**Quanta Computer Inc.**

**PROJECT : ZRP**

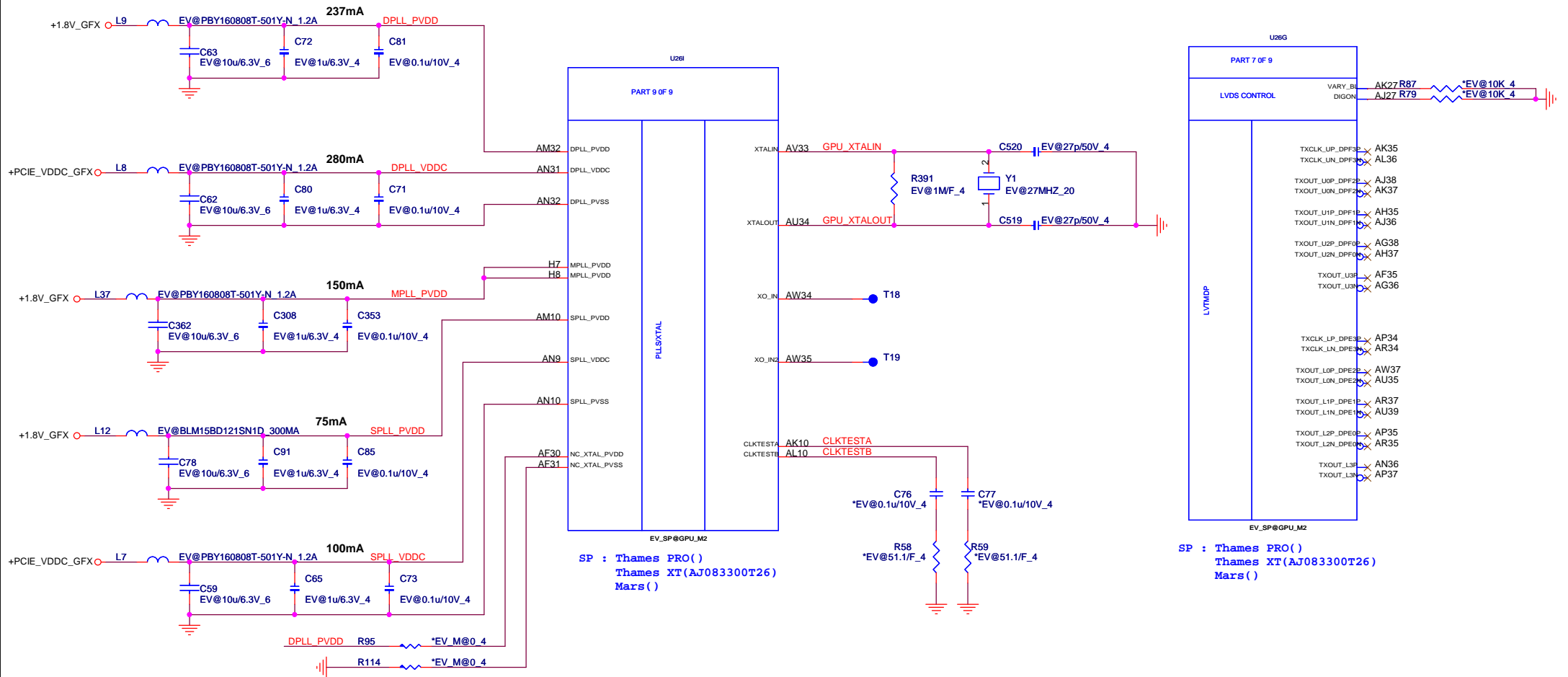
Size	Document Number	Rev
	<b>Thames_M2/ PEG*16</b>	<b>A1A</b>
Date:	Friday, June 01, 2012	Sheet 14 of 44



Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	



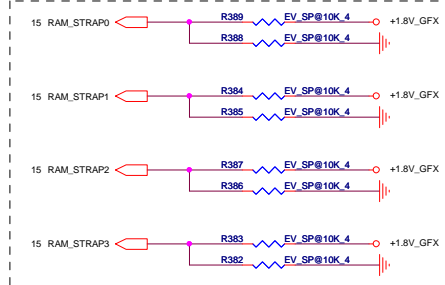


## Thames Pro,XT USE

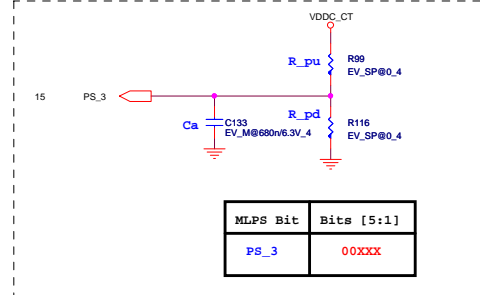
## Mars USE

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP3 DVPDATA_3	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0	MLPS
Hynix	H5TQ1G63DFR-11C (64M*16)	AKD5LZWTW05 * 8	1GB	0	0	0	0	000
	H5TQ2G63DFR-11C (128M*16)	AKD5MGWTW17 * 4	1GB	0	0	0	1	
		AKD5MGWTW17 * 8	2GB	0	0	1	0	
Samsung	K4W1G1646G-BC11 (64M*16)	AKD5EGGT500 * 8	1GB	0	1	0	0	010
	K4W2G1646G-HC11 (128M*16)	AKD5MGWT500 * 4	1GB	0	1	0	1	
		AKD5MGWT500 * 8	2GB	0	1	1	0	
AMD	23EY2387MC11 (64M*16)	AKD5EZWT700 * 8	1GB	1	0	0	0	100
	23EY4187MC11 (128M*16)	AKD5DZWT700 * 4	1GB	1	0	0	1	
		AKD5DZWT700 * 8	2GB	1	0	1	0	

## SP : Thames DDR3 Memory TYPE Set



## SP : Mars DDR3 Memory TYPE Set



## MLPS

R_pu	R_pd	Bits [3:1]
NC	4.75K	000
8.45K	2K	001
4.53K	2K	010
6.98K	4.99K	011
4.53K	4.99K	100
3.24K	5.62K	101
3.4K	1M	110
4.75K	NC	111

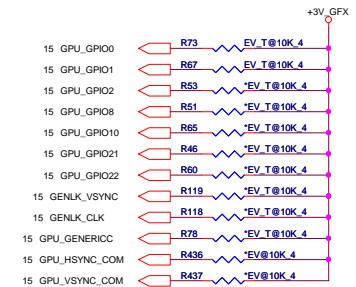
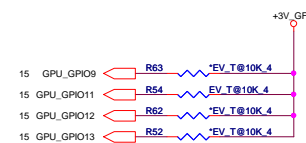
Ra	P/N
2K	CS22002FB19
3.24K	CS23242FB09
3.4K	CS23402FB08
4.53K	CS24532FB08
4.75K	CS24752FB12
4.99K	CS24992FB26
5.62K	CS25622FB18
6.98K	CS26982FB01
8.45K	CS28452FB12
1M	CS51002FB11

Ca	Bits [5:4]	P/N
680nF	00	CH4681K9B00
82nF	01	CH3823K1B00
10nF	10	CH31003KB11
NC	11	

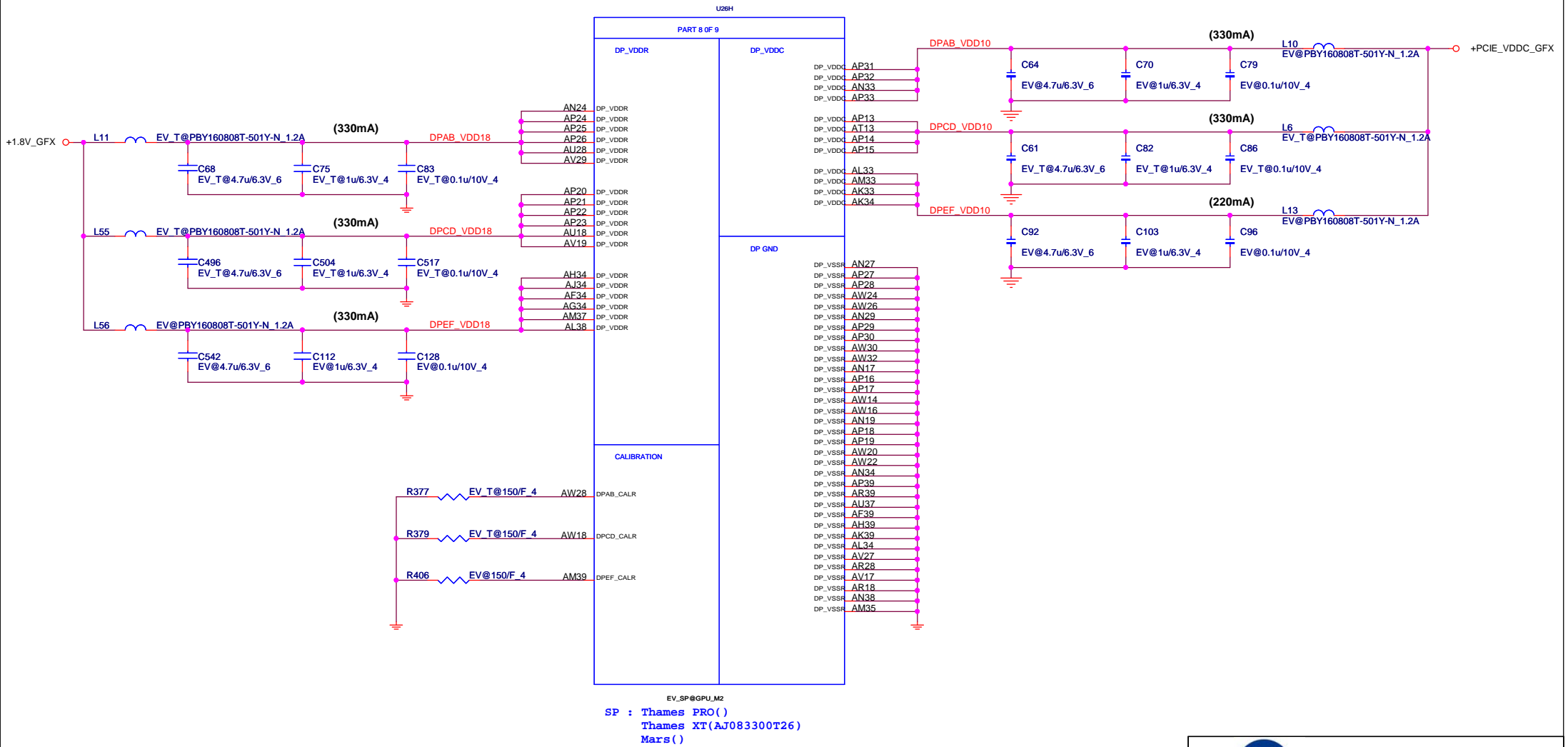
CONFIGURATION STRAPS -- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				Default Setting
STRAPS	MLPS	GPIO PIN	DESCRIPTION OF DEFAULT SETTINGS	
MLPS_DISABLE	NA	GPIO_28_FDO	Enable MLPS, NA for Thames/Whistler/Seymour 0: Enable MLPS, disable GPIO PINSTRAP 1: Disable MLPS, enable GPIO PINSTRAP	X
TX_PWRS_ENB	PS_1[4]	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X
TX_DEEMPH_EN	PS_1[5]	GPIO1	PCIe Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	X
BIF_GEN3_EN_A	PS_1[1]	GPIO2	PCIe Gen3 Enable (NOTE: RESERVED for Thames/Whistler/Seymour) 0: GEN3 not supported at power-on 1: GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	GPIO9	VGA Control 0: VGA controller capacity enabled 1: VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	PS_0[3..1]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select  If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 110 - 2Mbit M25P20 (ST) 111 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	XXX
BIOS_ROM_EN	PS_2[3]	GPIO22	Enable external BIOS ROM device 0: Disabled 1: Enabled	X
AUD[1] AUD[0]	NA NA	HSYNC VSYNC	00 - No audio function 01 - Audio for DP only 10 - Audio for DP and HDMI if dongle is detected 11 - Audio for both DP and HDMI HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	XX
CEC_DIS	PS_0[4]	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0: Disabled 1: Enabled	X
RESERVED RESERVED RESERVED	PS_1[3] PS_1[2] NA	GENLK_CLK GPIO8 GPIO21 GENERIC	NOTE: ALLOW FOR PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTOR IF THESE GPIOs ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET  Reserved Reserved Reserved Reserved (for Thames/Whistler/Seymour only)	0 0 0 0
AUD_PORT_CONN_PINSTRAP[2] AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[0]	PS_3[5] PS_3[4] PS_0[5]	NA NA NA	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX

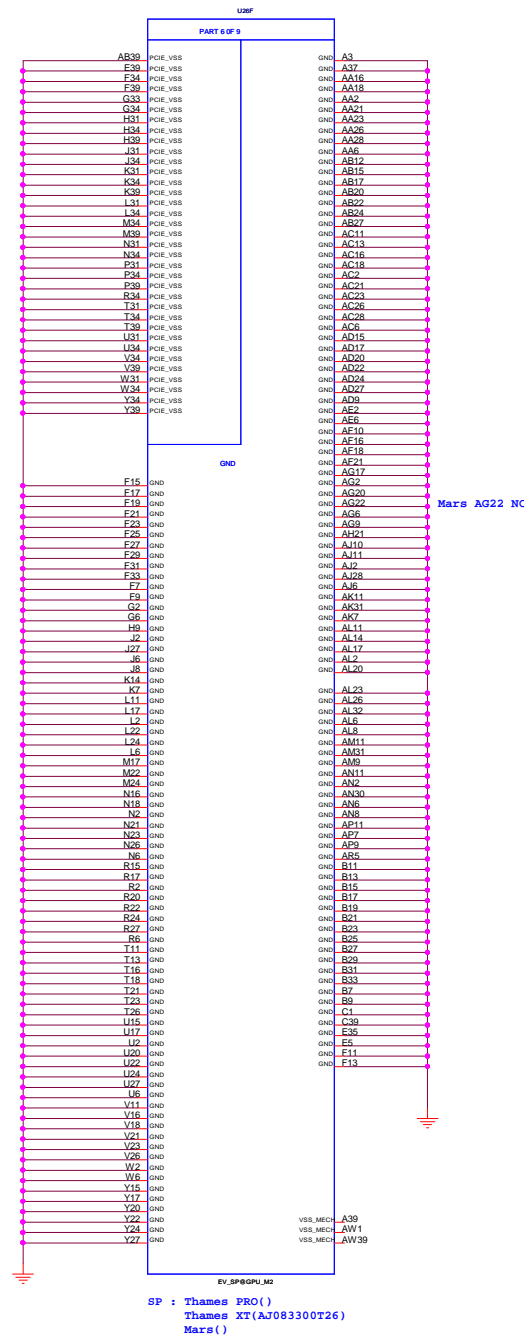
## System Memory Aperture size

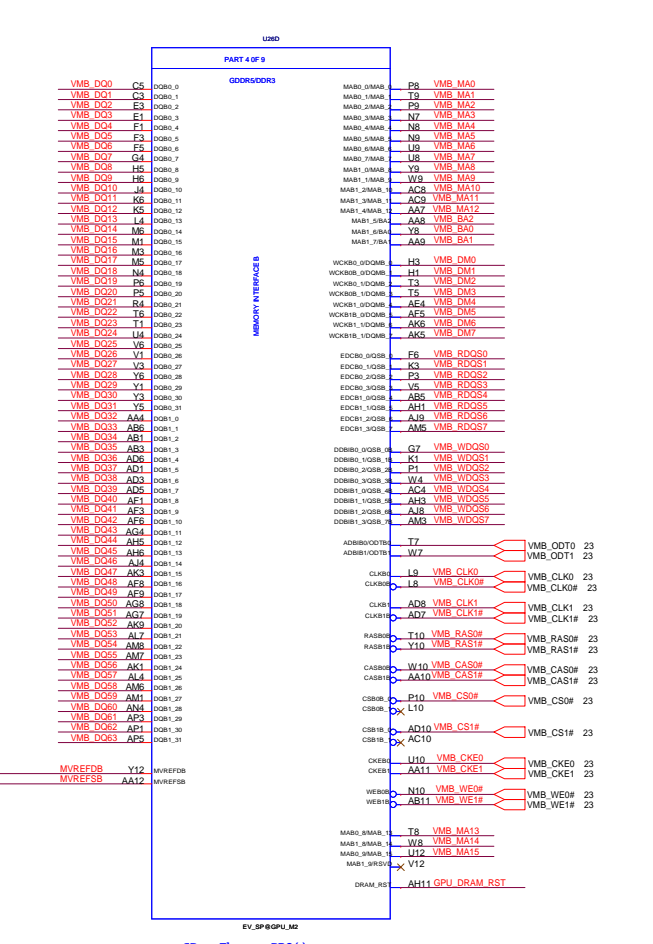
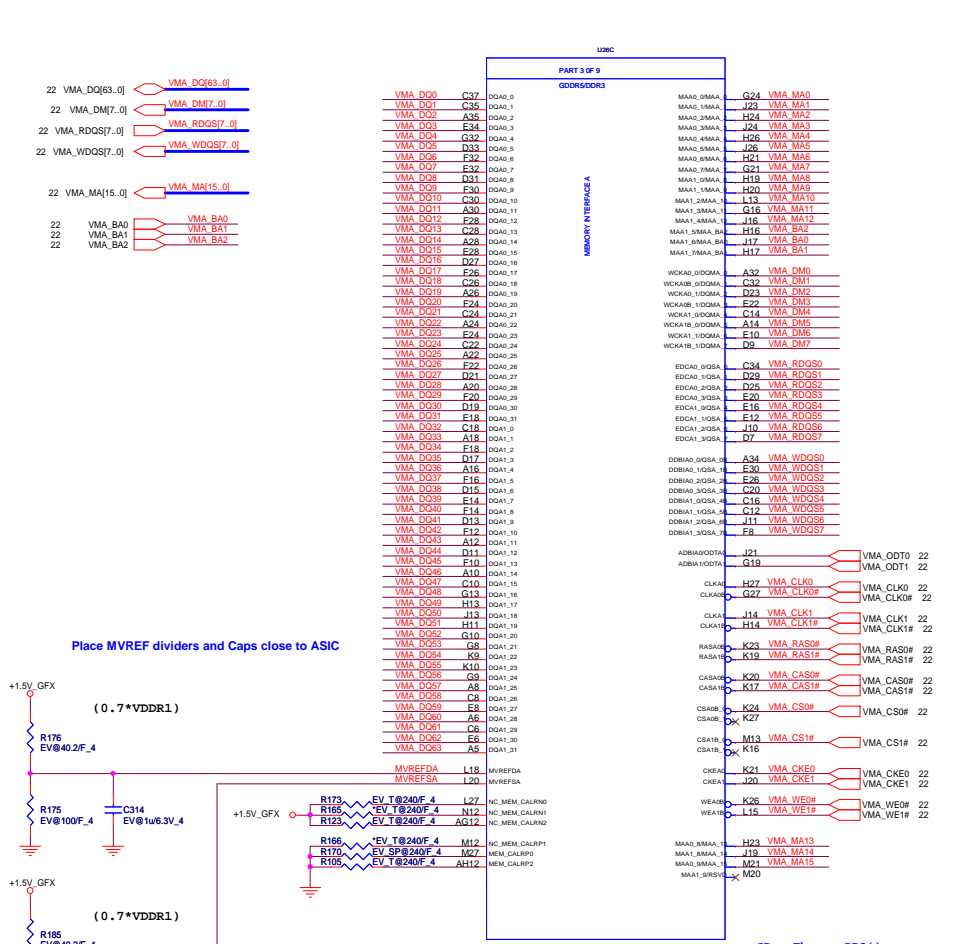
GPIO9 BIOSROM		GPIO11 ROMIDCFG0	GPIO12 ROMIDCFG1	GPIO13 ROMIDCFG2
0	128M	0	0	0
0	256M	1	0	0
0	64M	0	1	0
0	32M	1	1	0





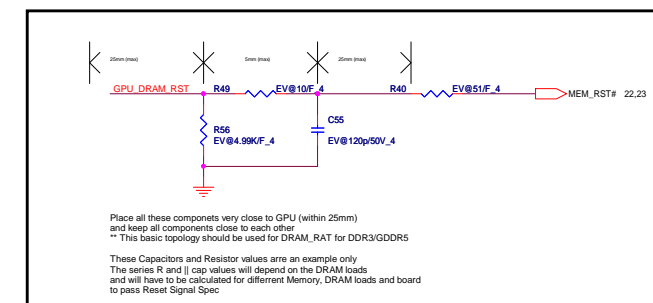






SP : Thames Pro,XT R=240ohm(CS12402FB00)  
Mars R=120ohm(CS11202FB11)

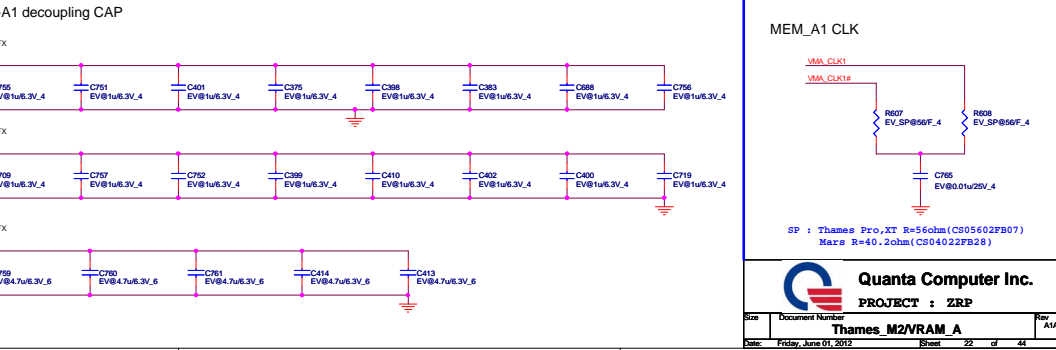
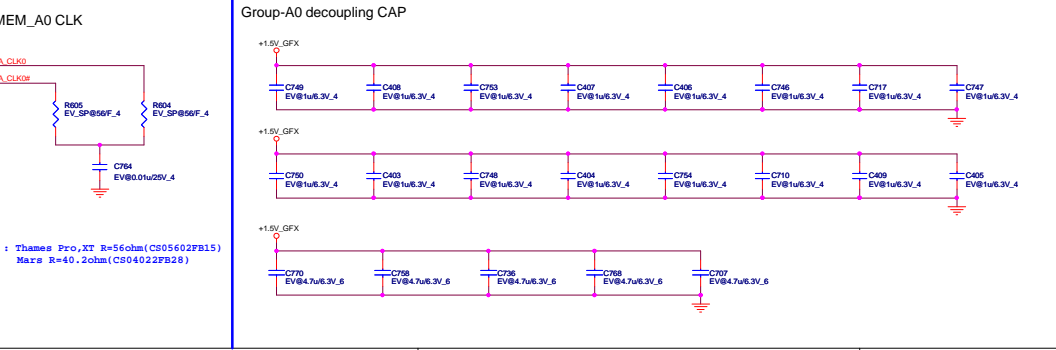
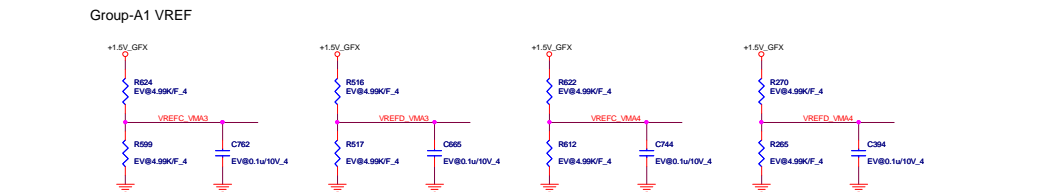
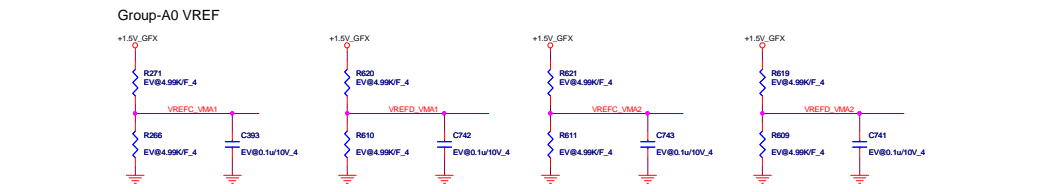
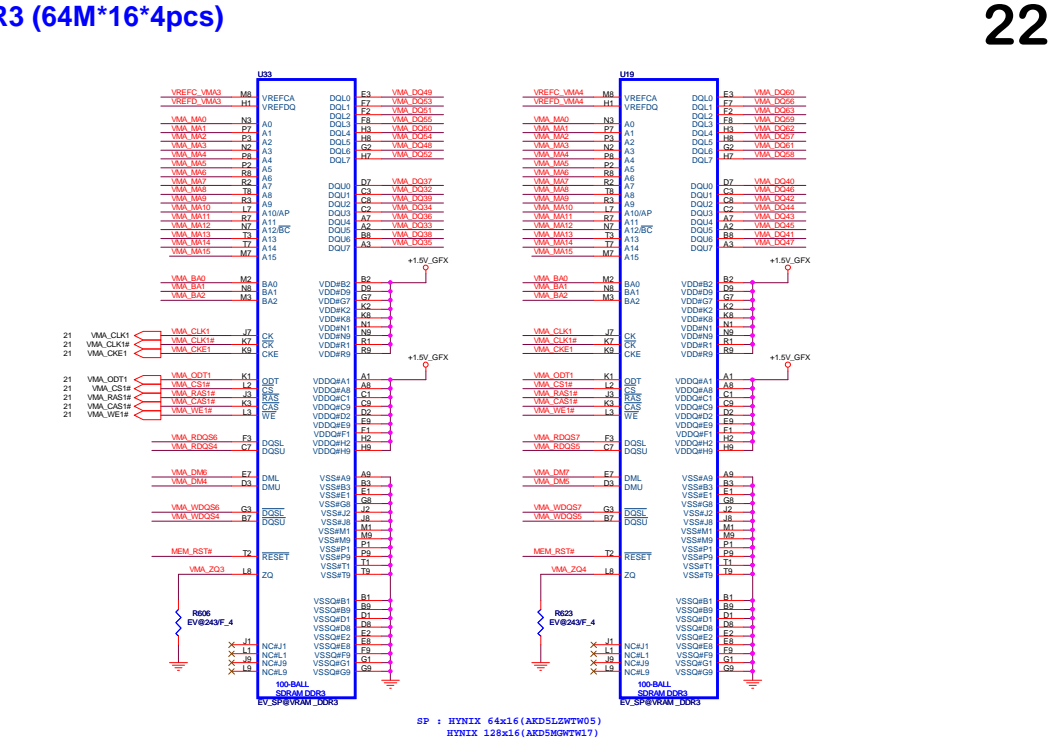
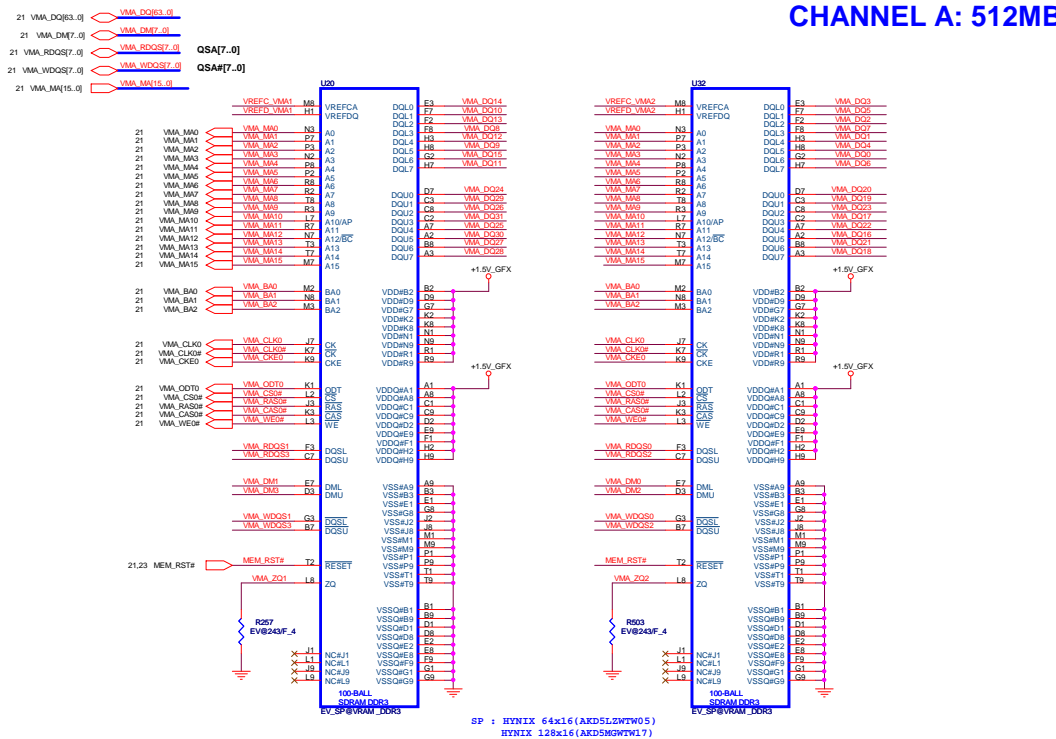
Ball Name	Thames	Mars
MEM_CALRN0	240ohm	X
MEM_CALRN1	X	X
MEM_CALRN2	240ohm	X
MEM_CALRP0	240ohm	120ohm
MEM_CALRP1	X	X
MEM_CALRP2	240ohm	X



Place all these components very close to GPU (within 25mm) and keep all components close to each other  
 \*\* This basic topology should be used for DRAM\_RST for DDR3/GDDR5

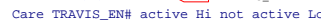
These Capacitors and Resistor values are an example only  
 The series R and if cap values will depend on the DRAM loads and will have to be calculated for different Memory, DRAM loads and board to pass Reset Signal Spec

# CHANNEL A: 512MB DDR3 (64M\*16\*4pcs)

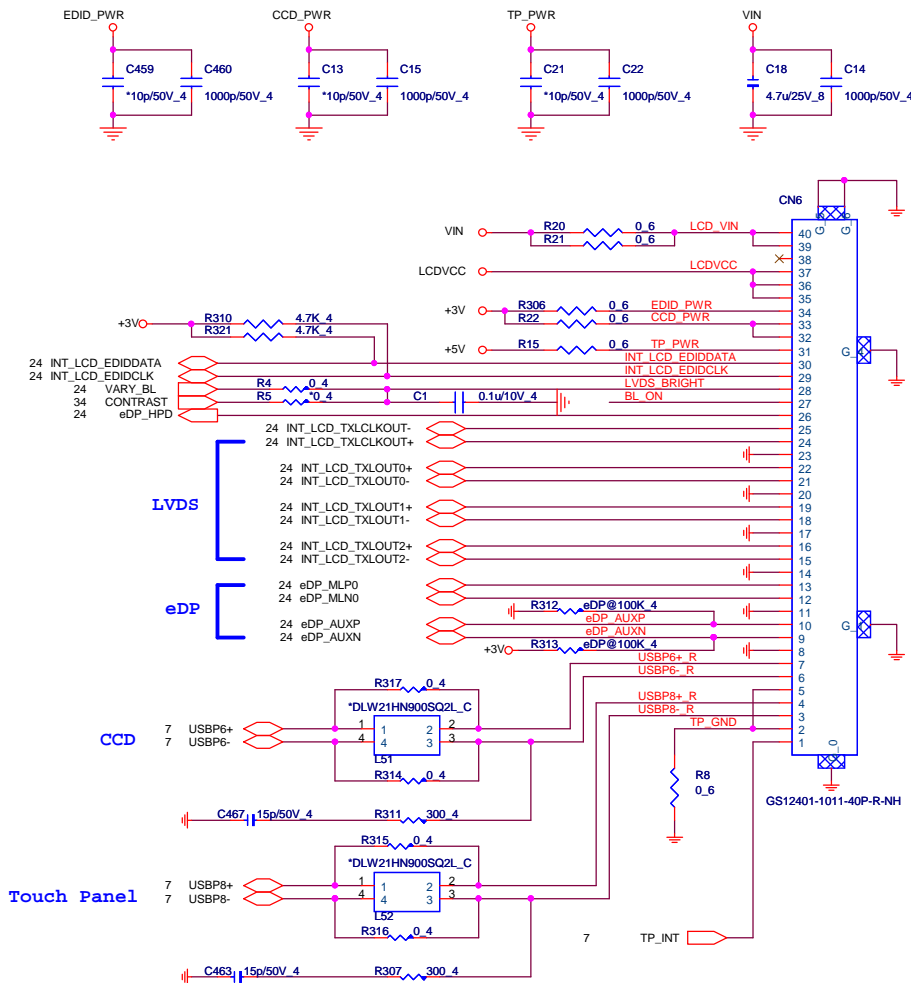




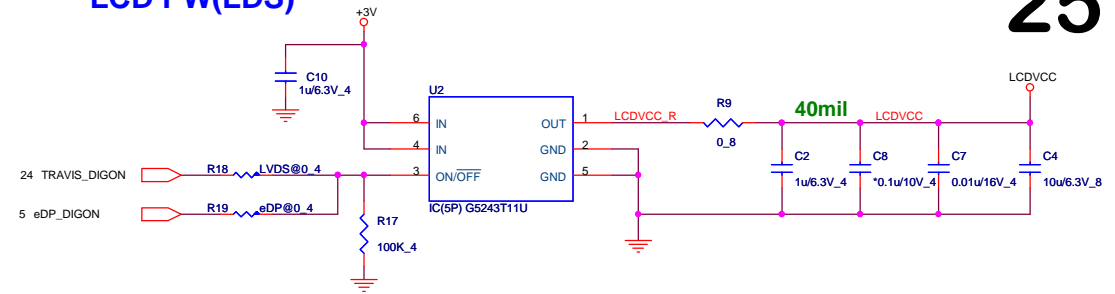




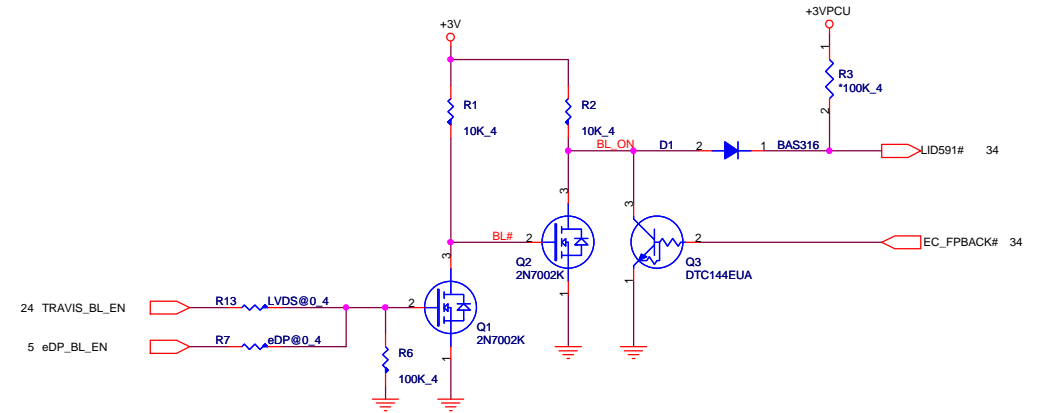
## LVDS(LDS)



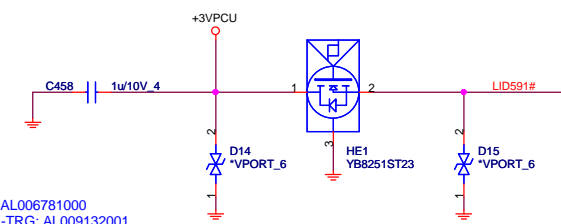
## LCD PW(LDS)



## Backlight Control(LDS)

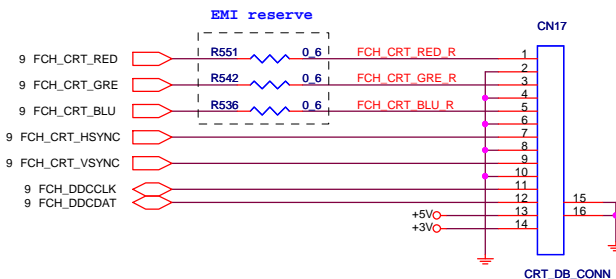


## Lid Switch (HSR)

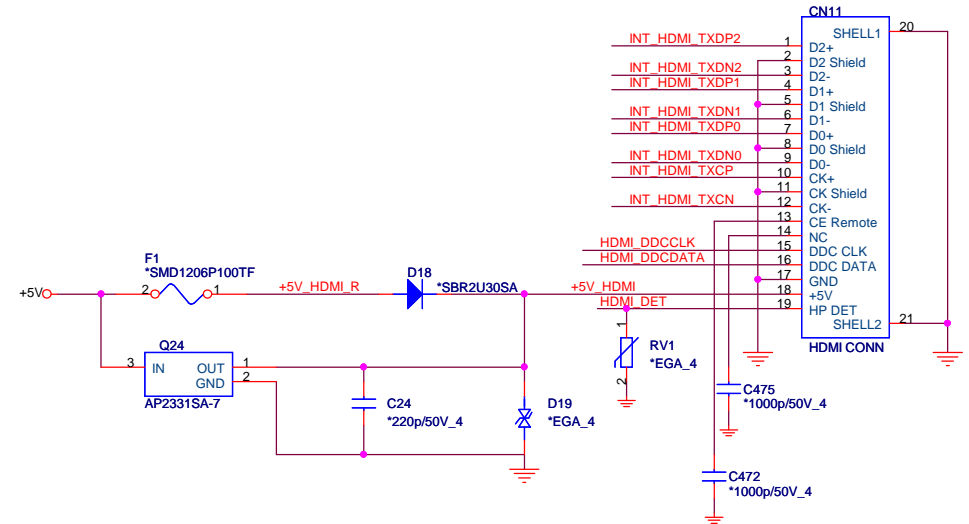
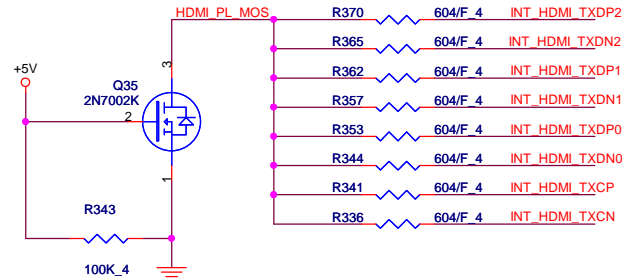
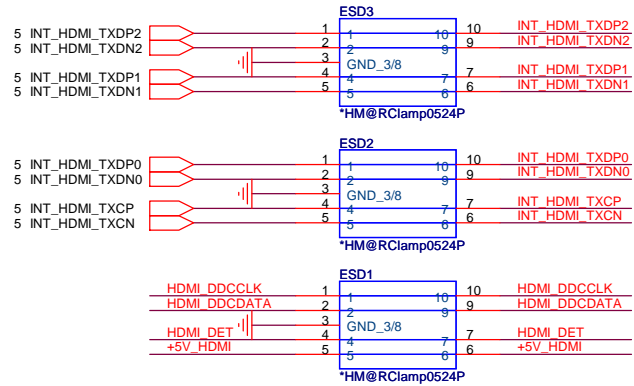


EM-6781-T3: AL006781000  
APX9132H AI-TRG: AL009132001  
AH9249NTR-G1: AL009249000

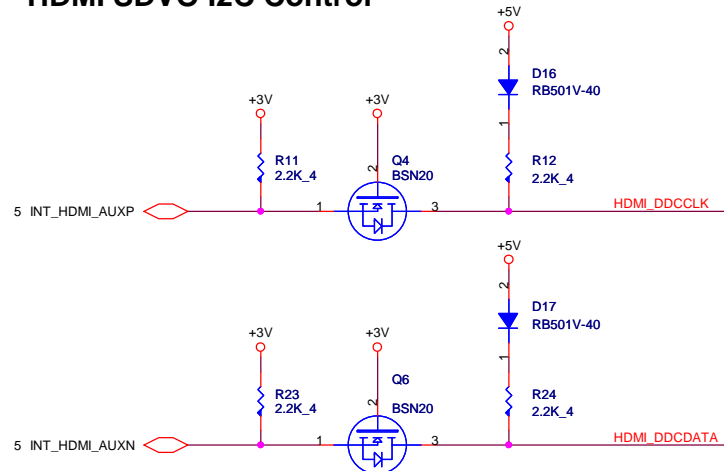
## CRT DB



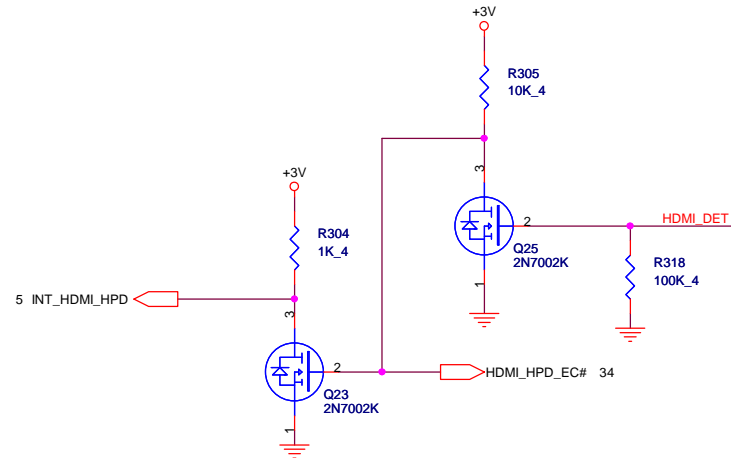
ESD



## HDMI SDVO I2C Control

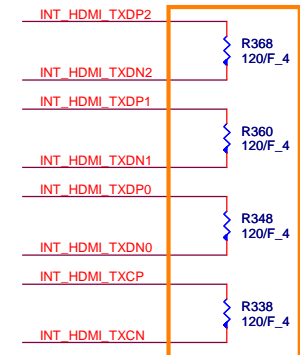


## HDMI HPD SENSE



## EMI reserve for HDMI(EMC)

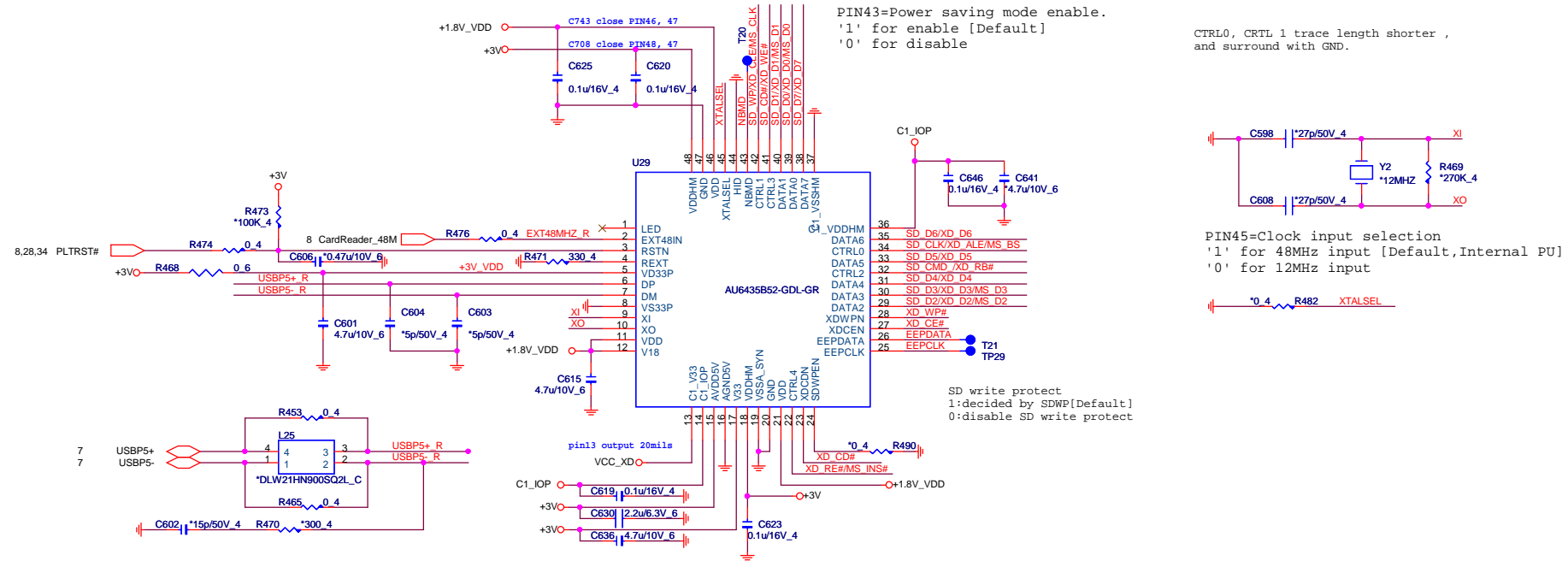
Close connector



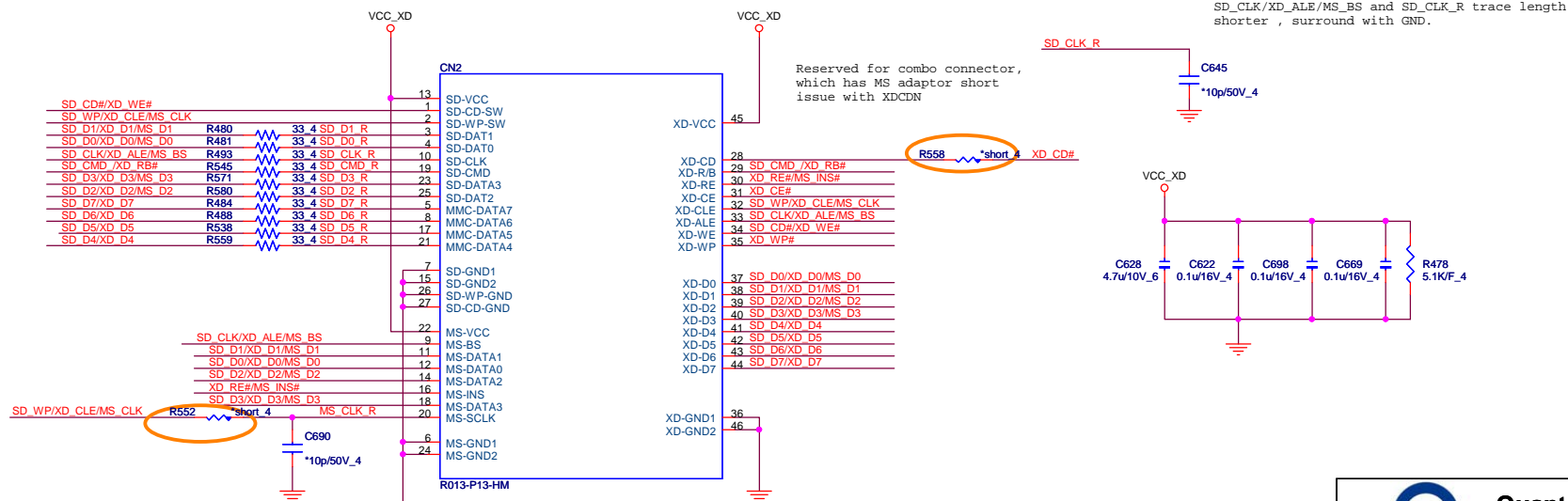
Quanta Computer Inc.

PROJECT : ZRP

Size	Document Number	Rev
	HDMI	A1A
Date:	Friday, June 01, 2012	Sheet 26 of 44



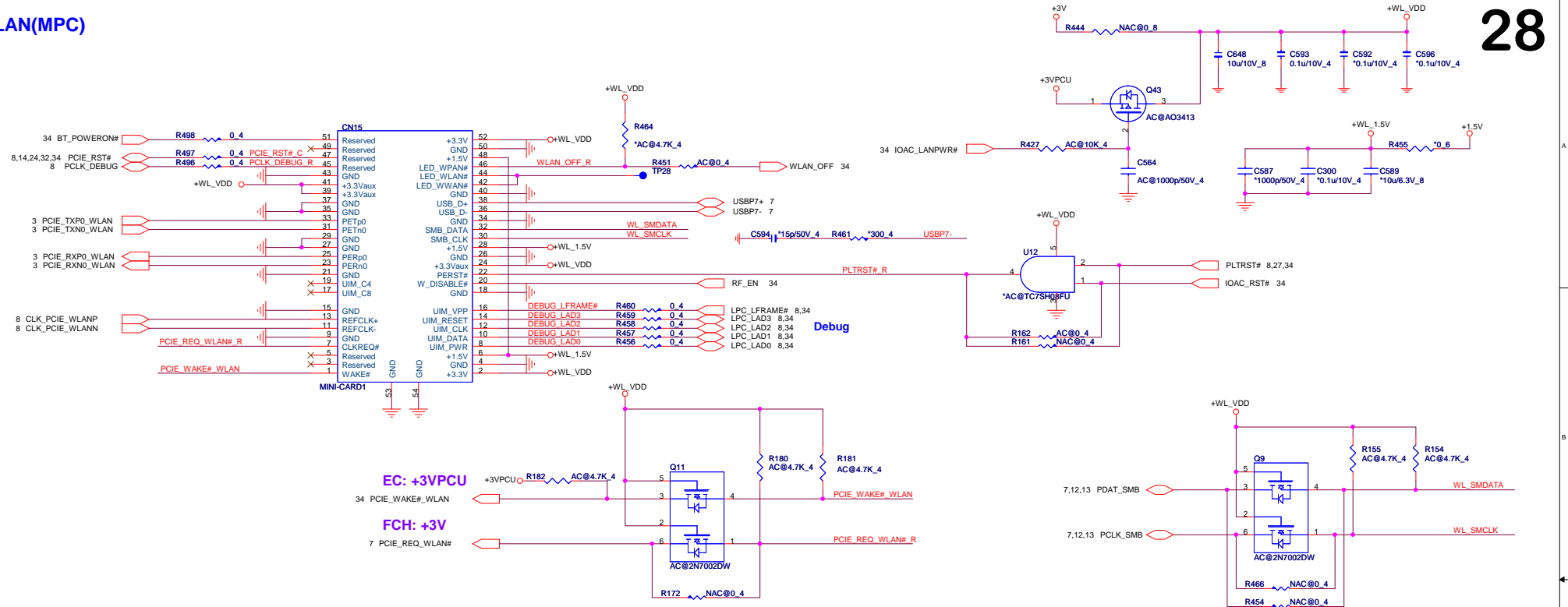
## 5 IN 1 CARD READER CONN (SD/MMC)



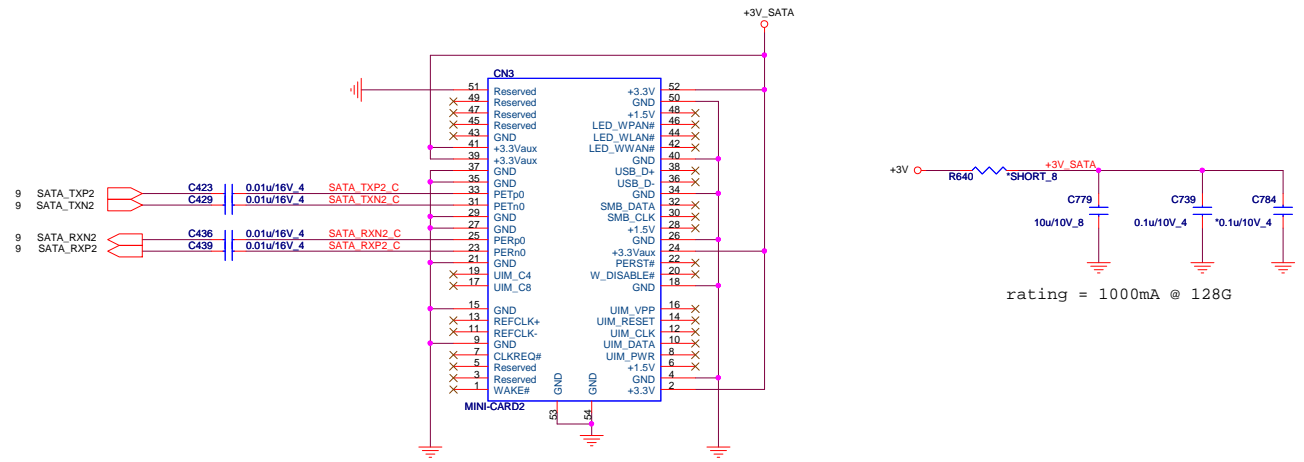
SD\_WP/XD\_CLE/MS\_CLK and MS\_CLK\_R trace length  
shorter , surround with GND.

# MINI-CARD WLAN(MPC)

+3.3V: 1000mA  
+3.3Vaux: 330mA  
+1.5V: 500mA

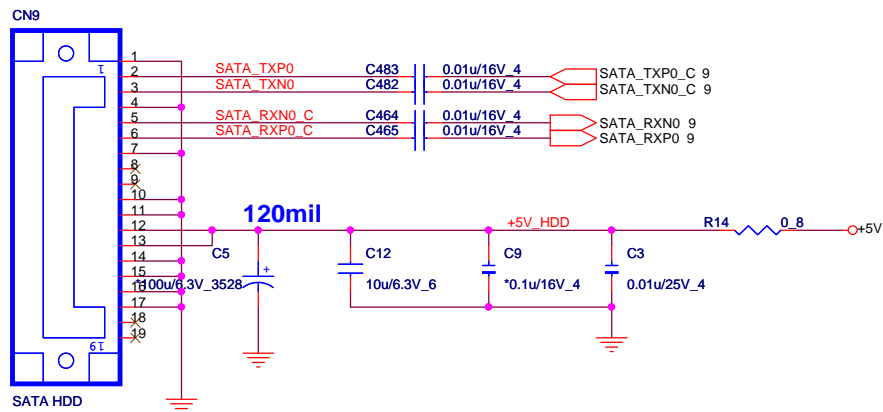


# MINI-CARD SSD

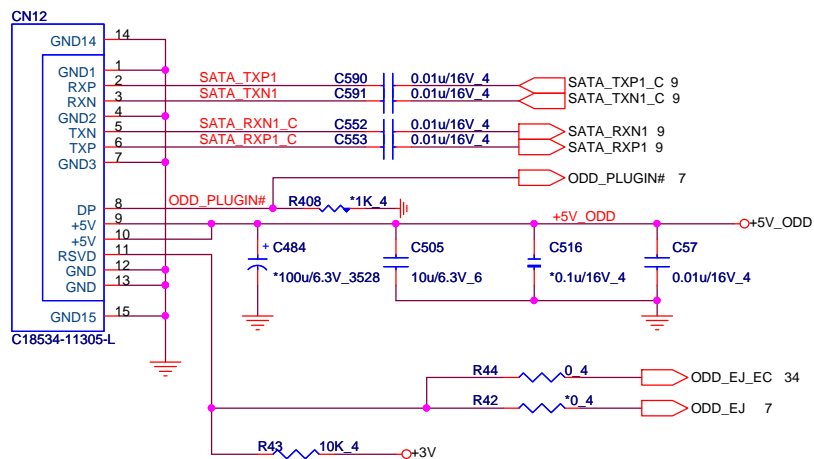


rating = 1000mA @ 128G

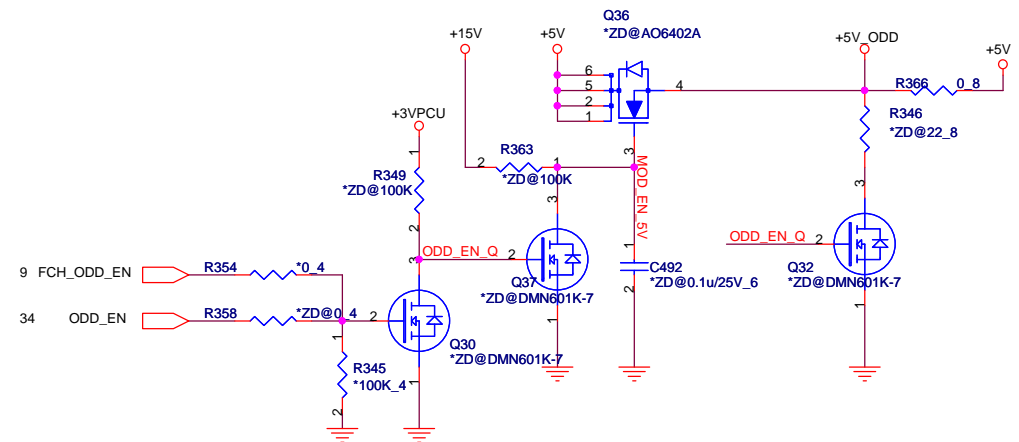
## SATA HDD



## SATA ODD



## Zero Power (ODD)



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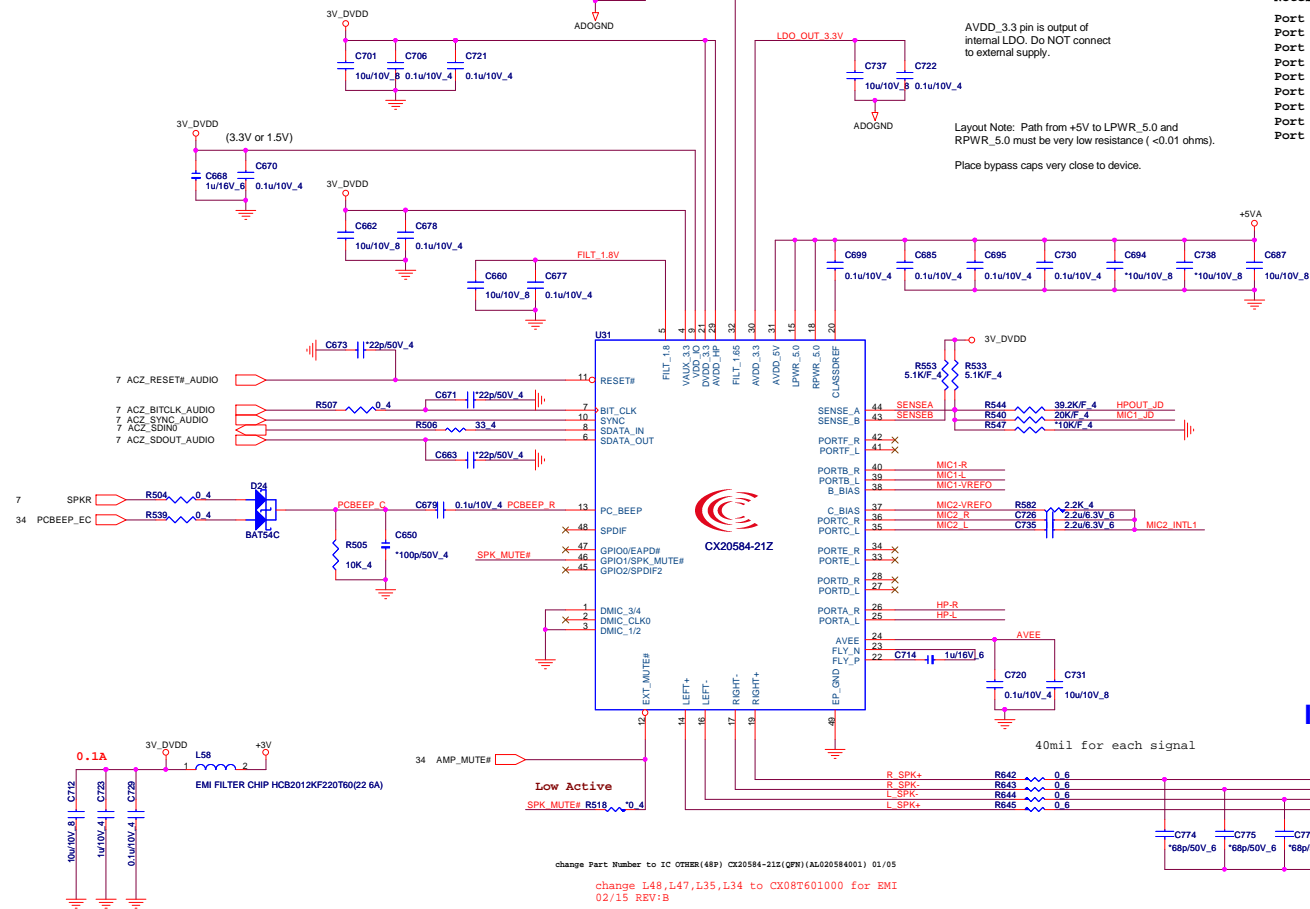
**PROJECT : ZRP**

Size	Document Number	Rev
	<b>SATA(HDD/ODD)</b>	A1A

Date: Friday, June 01, 2012 Sheet 29 of 44



## AUDIO CODEC

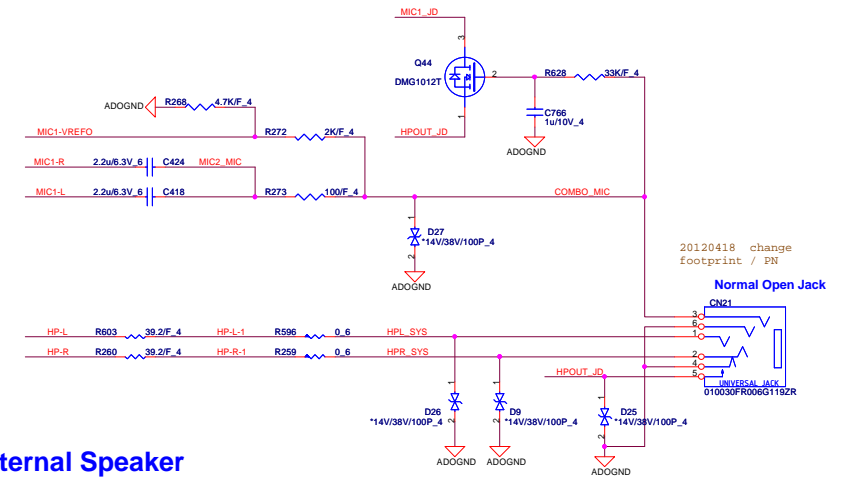


## Port Configuration

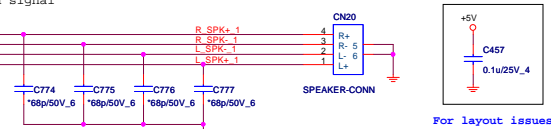
**Notes:**

- Port A: Headphone jack (jack shared with S/PDIF)
- Port B: Internal MIC (mono or stereo)
- Port C: Microphone/LI/LO jack
- Port D: Line Out jack (Optional)
- Port E: Line In jack (Optional)
- Port F: Not used.
- Port G: Internal stereo speakers
- Port J: Internal stereo digital mic (Optional)
- Port H: S/PDIF (jack shared with headphone)

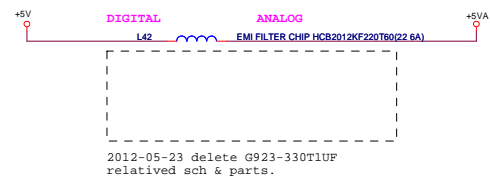
## HEADPHONE/Mic combo



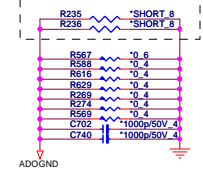
## Internal Speaker



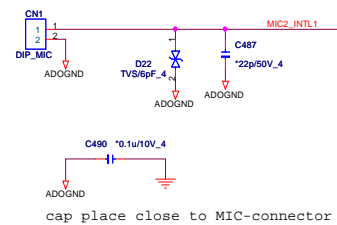
## Power (ADO)



2012-05-23 Add short pad for vendor suggestion.

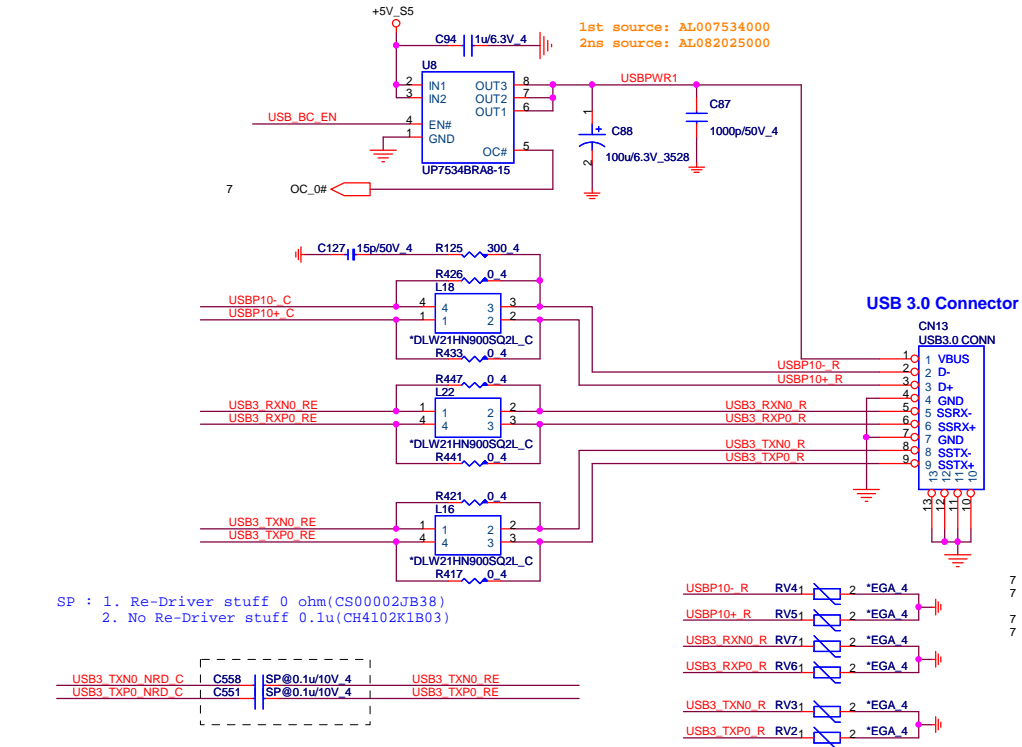


## INT DIP AMIC array



1. The VDD\_IO and VAUX\_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
2. To support Wake-on-Jack, the codec VAUX\_3.3 pin must be powered from a Standby supply.
3. C309, C310, C311 are optional. Do not install unless needed for EMI/SI.

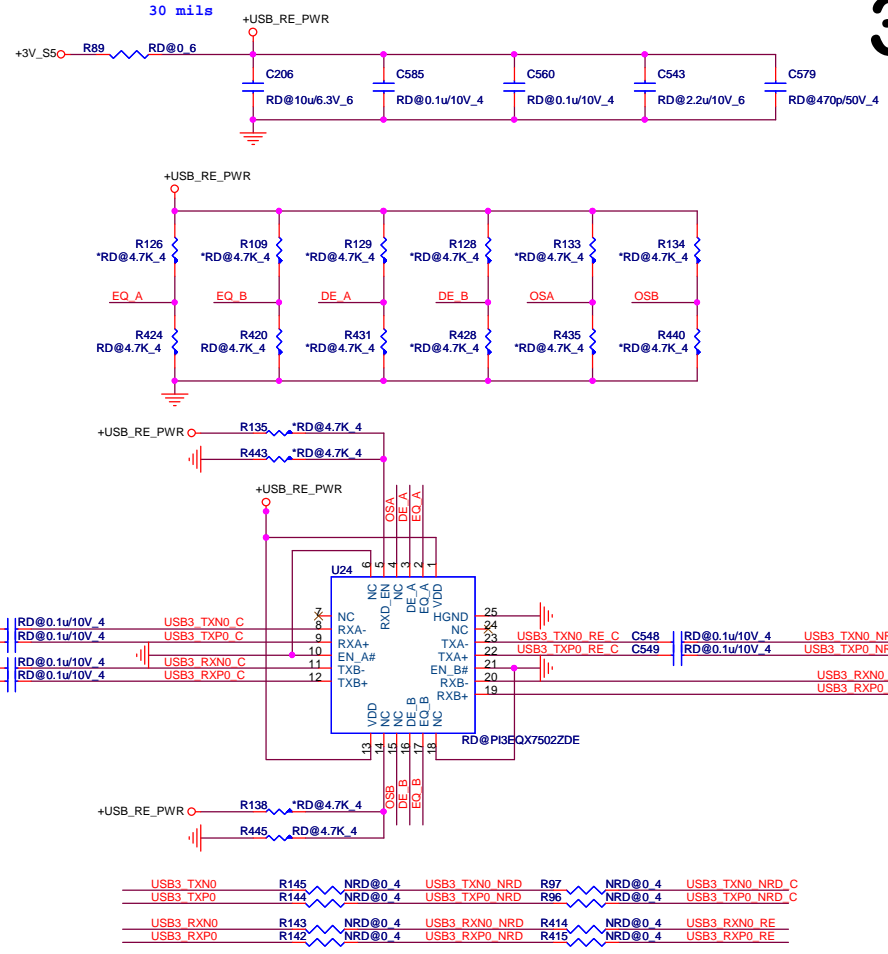
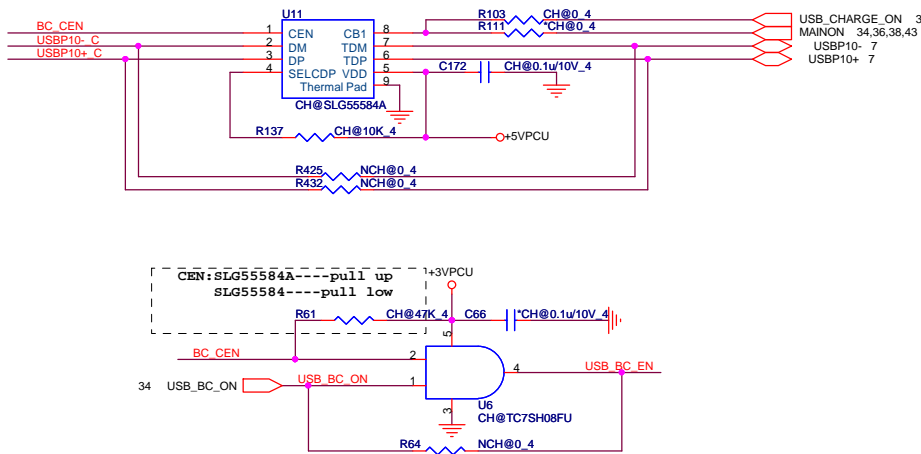
PROJECT : ZRP			
Size	Document Number	Rev	
	<b>CONEXANT 20584</b>	1A	
Date	Friday, June 01, 2012	Sheet	30 of 44



SP : 1. Re-Driver stuff 0 ohm(CS00002JB38)  
2. No Re-Driver stuff 0.1u(CH4102K1B03)

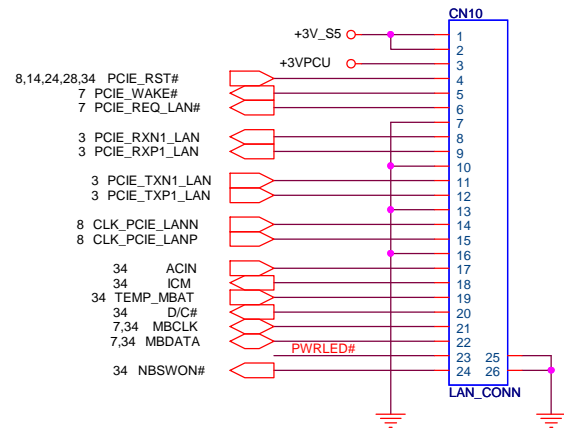
USB Charger to 3.0

CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

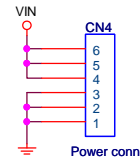


EXT. USB(USB)

## LAN& Charger DB



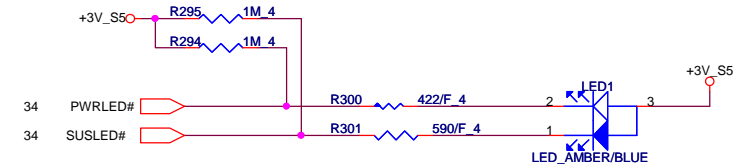
## POWER M/B (DCD)



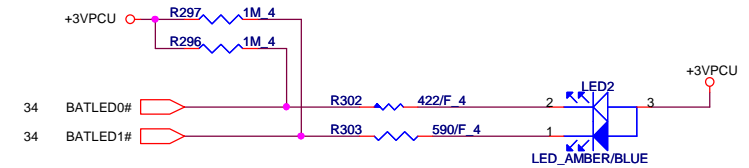
## LED(UIF)

32

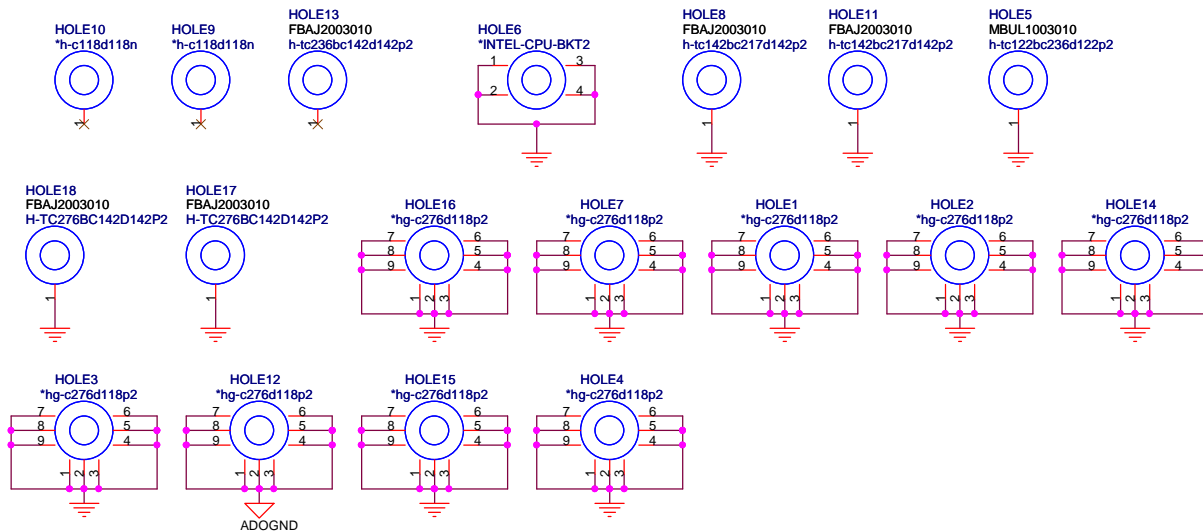
### Power




### Battery



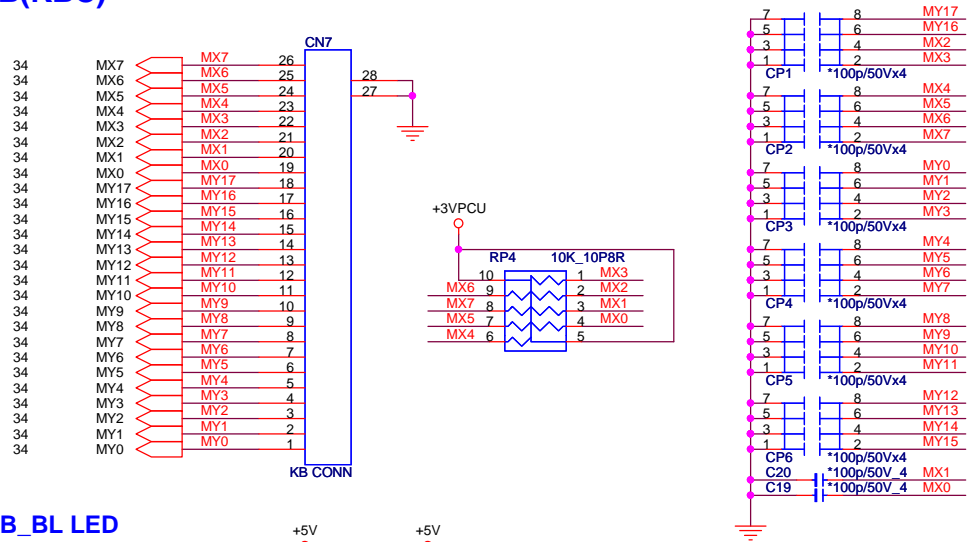
## HOLE(OTH)



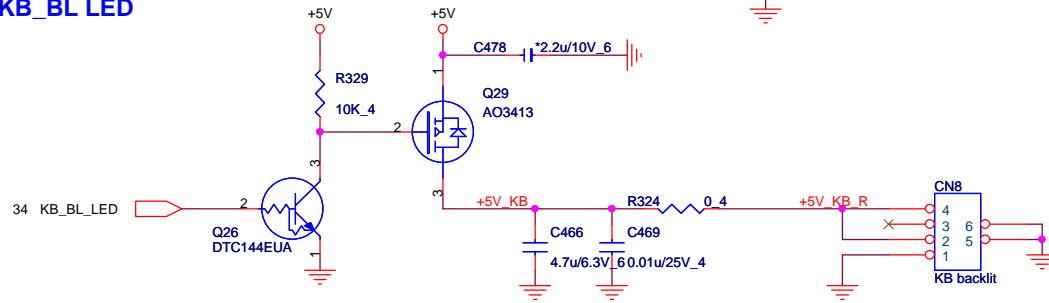
## EE RETURN-PATH CAPACITORS(EMC)

 <b>Quanta Computer Inc.</b> <b>PROJECT : ZRP</b>		Size	Document Number	Rev
		<b>LAN DB/ LED/ EMC/ Hole</b> Date: Friday, June 01, 2012		Sheet 32 of 44 Rev A1A

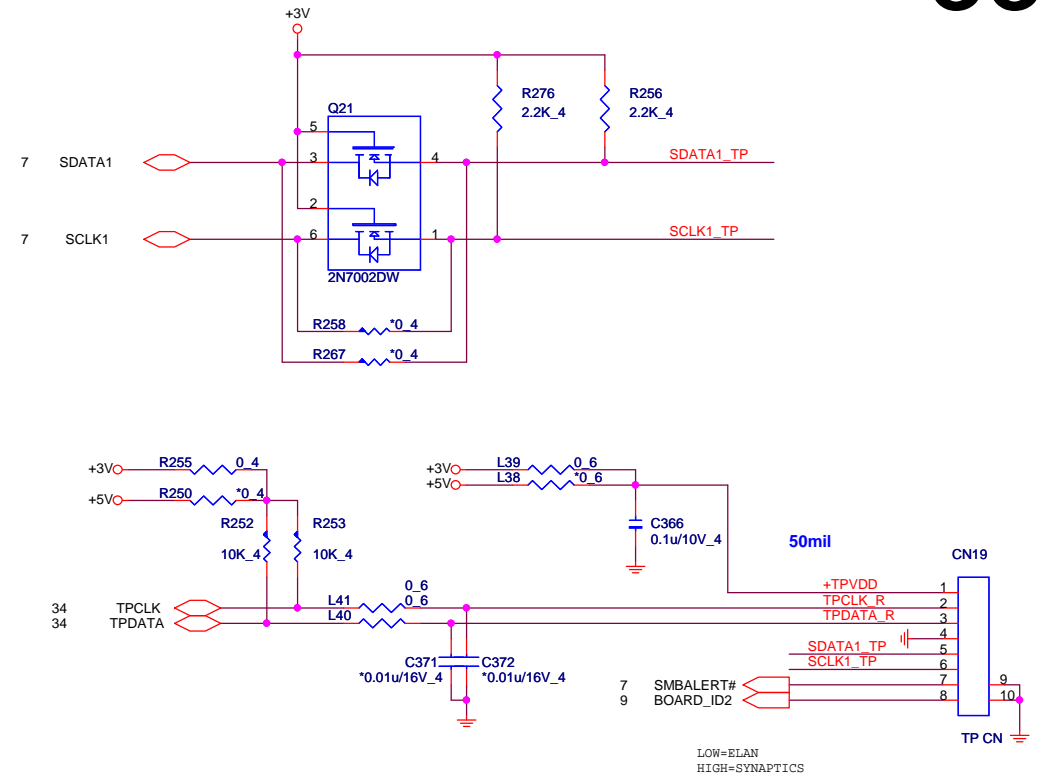
## K/B(KBC)



## KB\_BL LED

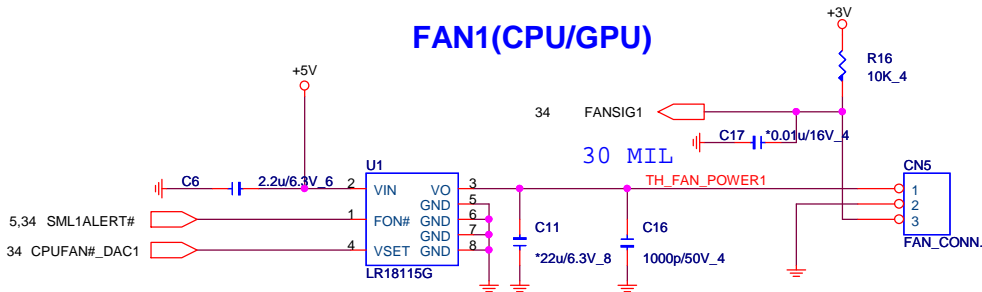


## TOUCHPAD BOARD CONN(TPD)

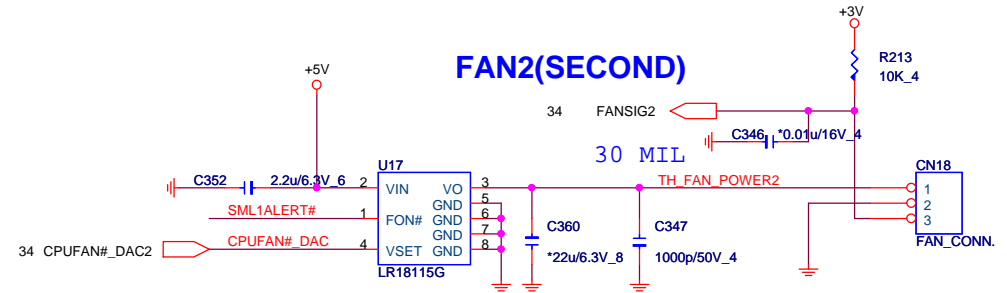


## CPU FAN(THM)

## FAN1(CPU/GPU)



## FAN2(SECOND)

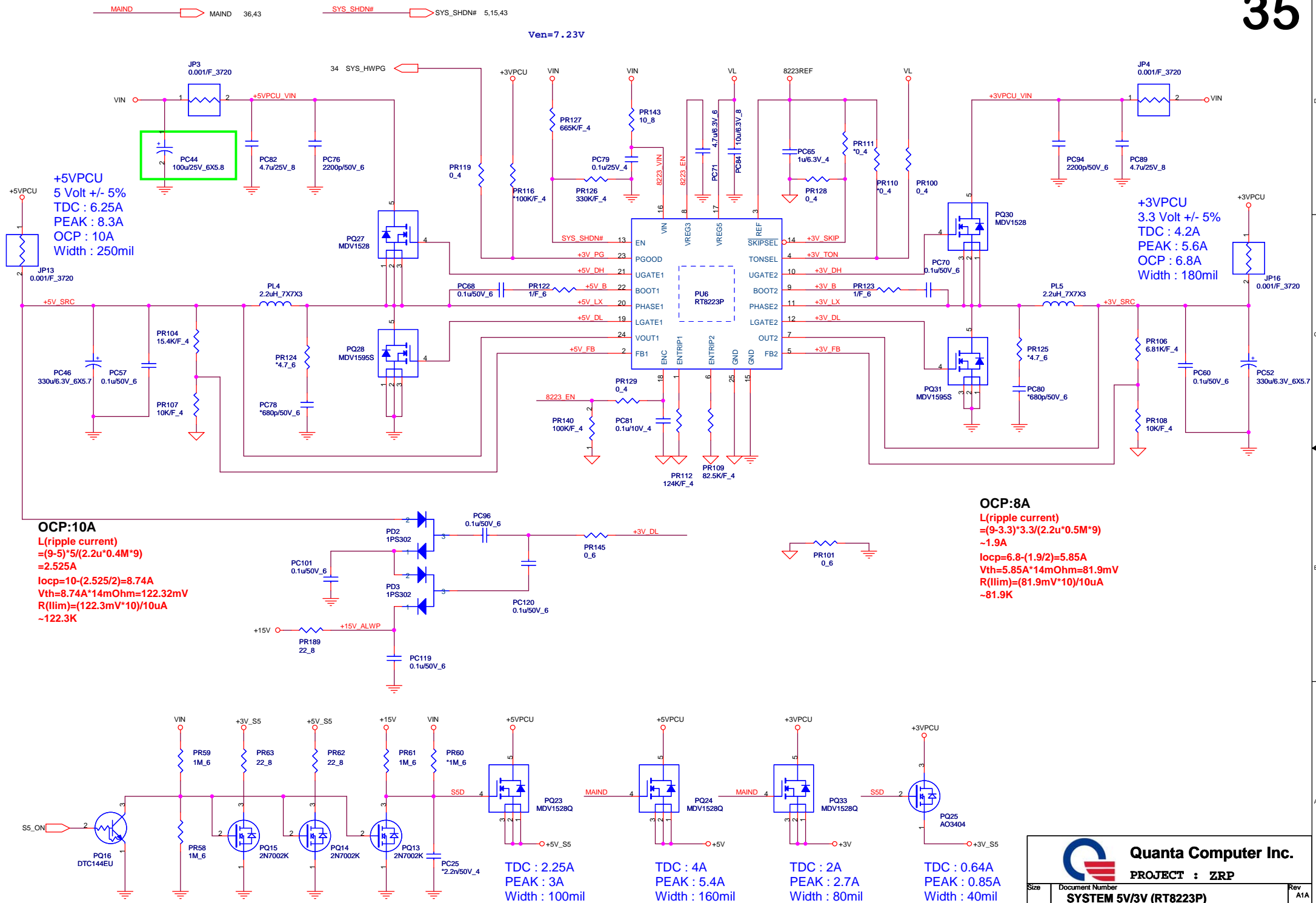


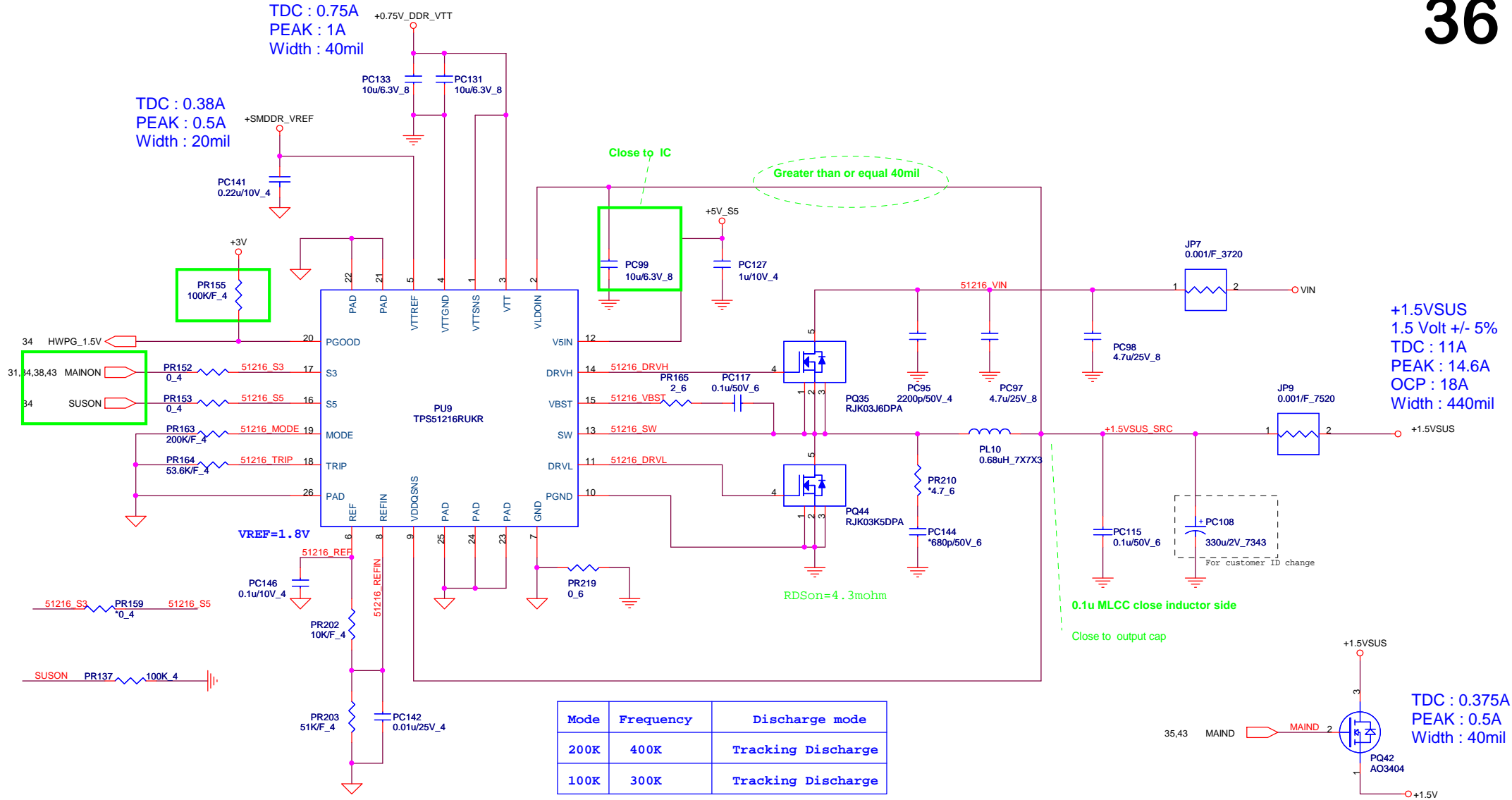
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PROJECT : ZRP

Size	Document Number	Rev
	KB/TP/FAN	A1A
Date:	Friday, June 01, 2012	Sheet 33 of 44







OCP=18A  
 L ripple current  
 $= (19-1.5) \times 1.5 / (0.68 \mu\text{s} \times 400 \text{K} \times 19)$   
 $= 5.079 \text{A}$   
 $V_{\text{trip}} = 18 - (5.079 / 2) \times 4.3 \text{mohm}$   
 $= 0.06647 \text{V}$   
 $R_{\text{limit}} = 0.06647 / 10 \mu\text{A} \times 8 \sim 53.183 \text{Kohm}$

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

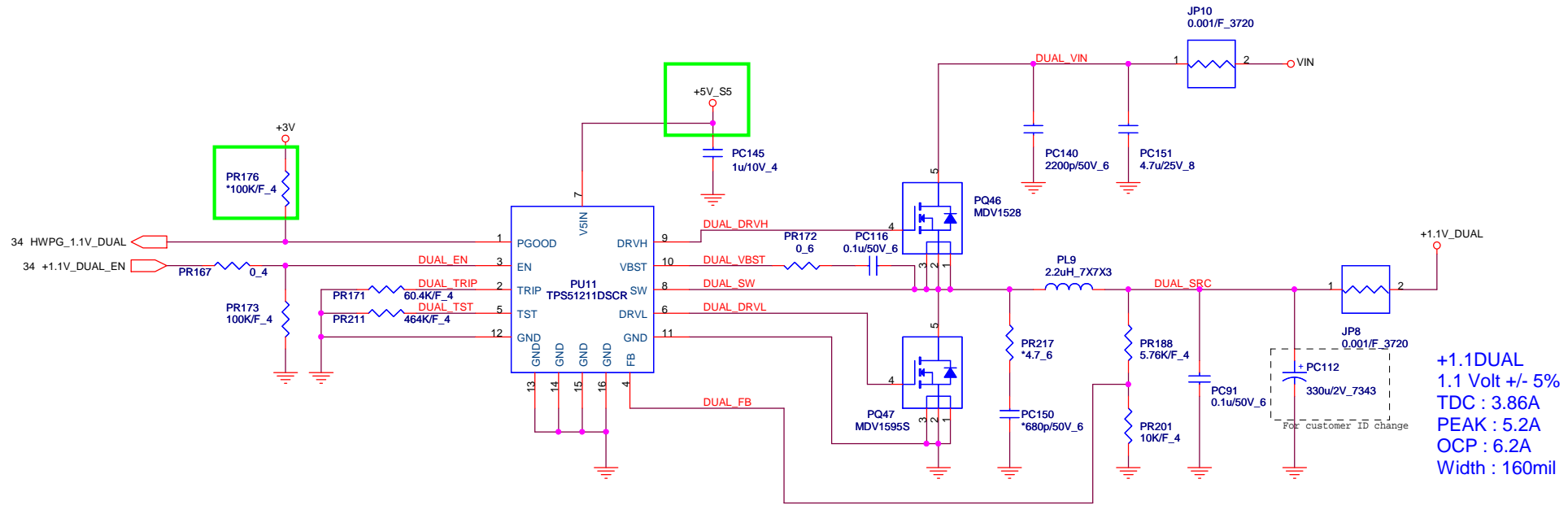
**Quanta Computer Inc.**  
**PROJECT : ZRP**

Size   Document Number   Rev

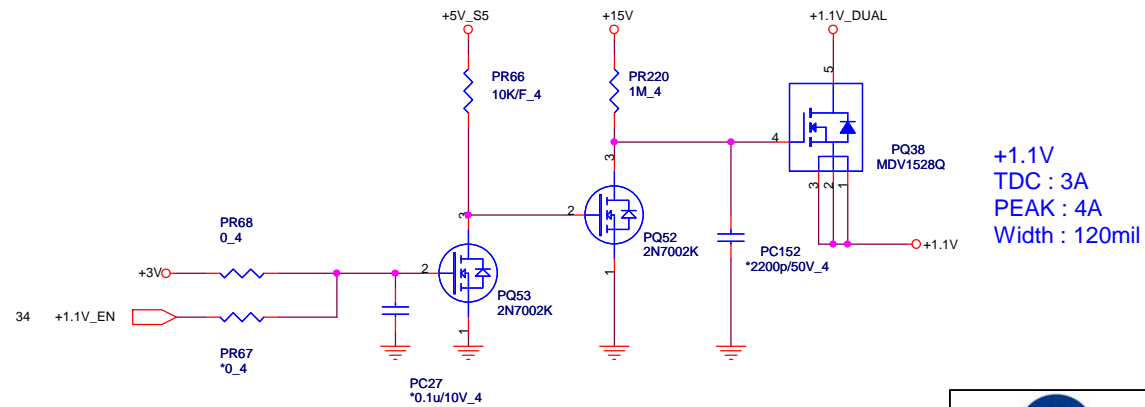
**DDR 1.5V(TPS51216)**   A1A

Date: Friday, June 01, 2012   Sheet 36 of 44





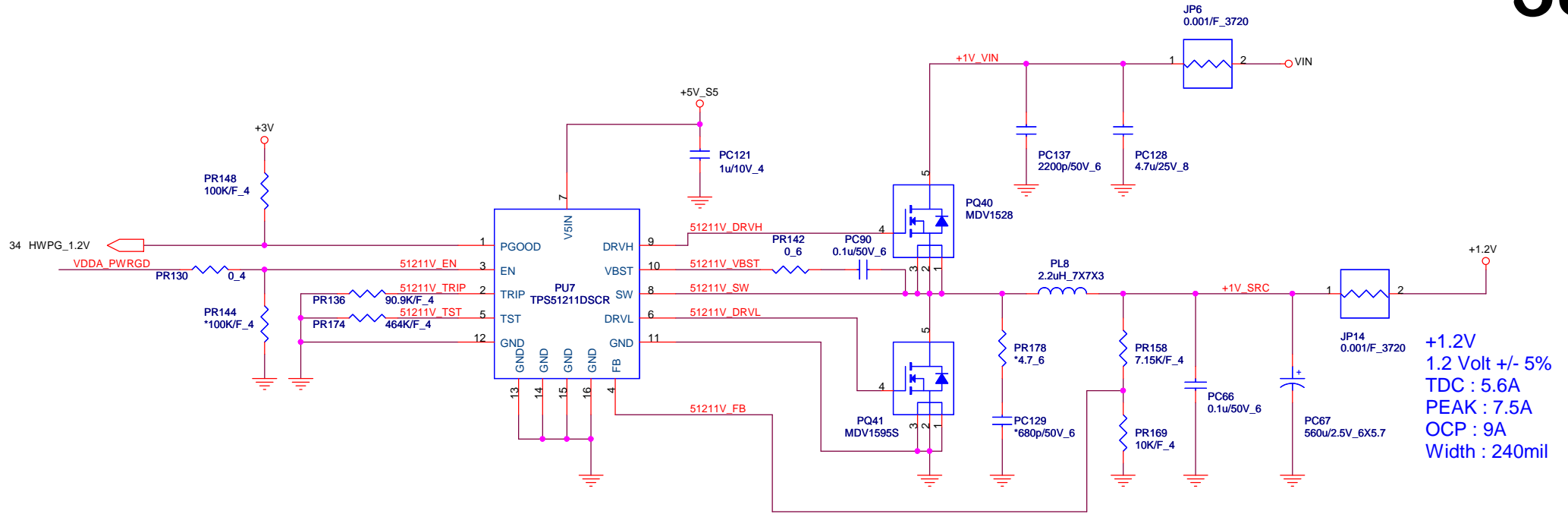
OCP=5A  
 L ripple current  
 $= (19-1.1) \times 1.1 / (2.2 \times 290 \times 19)$   
 $= 1.624A$   
 $V_{trip} = 6.2 - (1.624/2) \times 14mohm$   
 $= 0.07542V$   
 $R_{limit} = 0.07542 / 10uA \times 8 - 60.34Kohm$



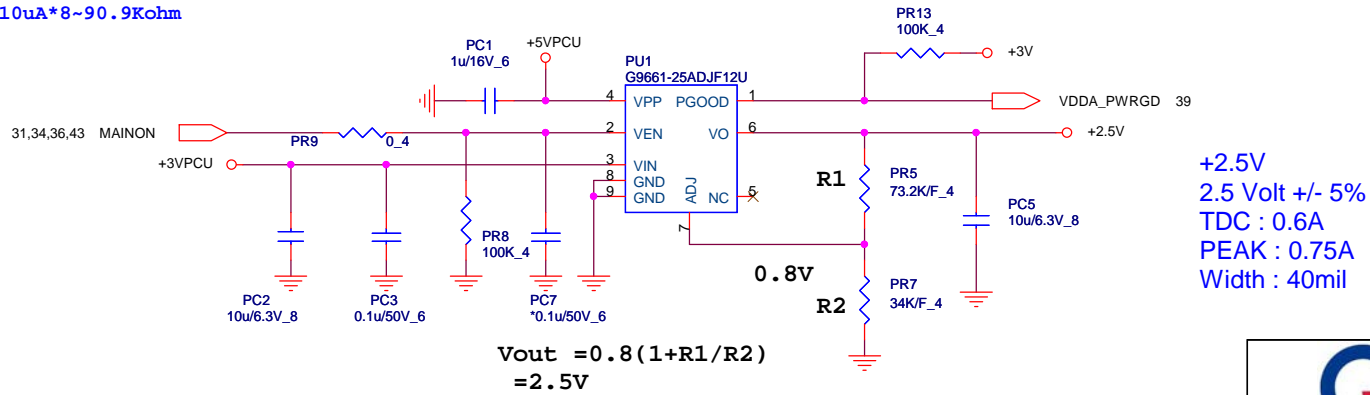
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**PROJECT : ZRP**

Size	Document Number	Rev
	<b>+1.1V_DUAL(TPS51211)</b>	A1A
Date:	Friday, June 01, 2012	Sheet 37 of 44



OCP=9A  
 L ripple current  
 $= (19 - 1.2) \times 1.05 / (2.2 \times 290 \times 19)$   
 $= 1.762A$   
 $V_{trip} = 9 - (1.762 / 2) \times 14 \text{mohm}$   
 $= 0.1136V$   
 $R_{limit} = 0.1136 / 10 \mu A \times 8 \sim 90.9 \text{Kohm}$



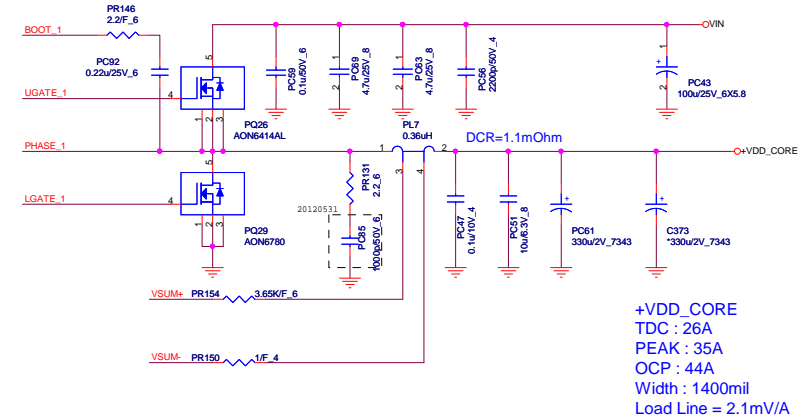
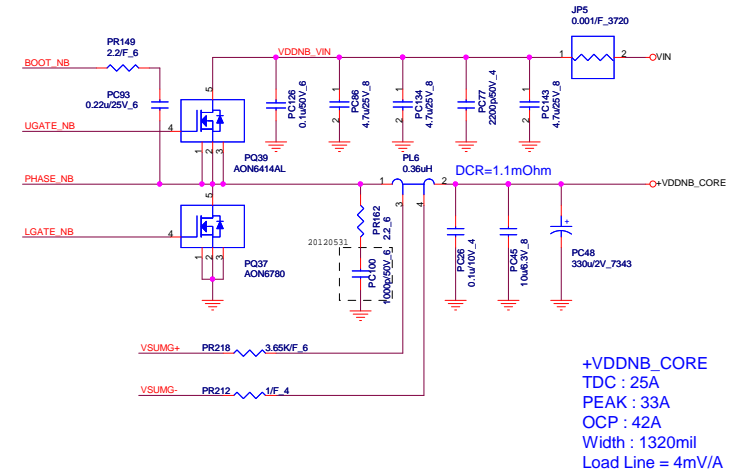
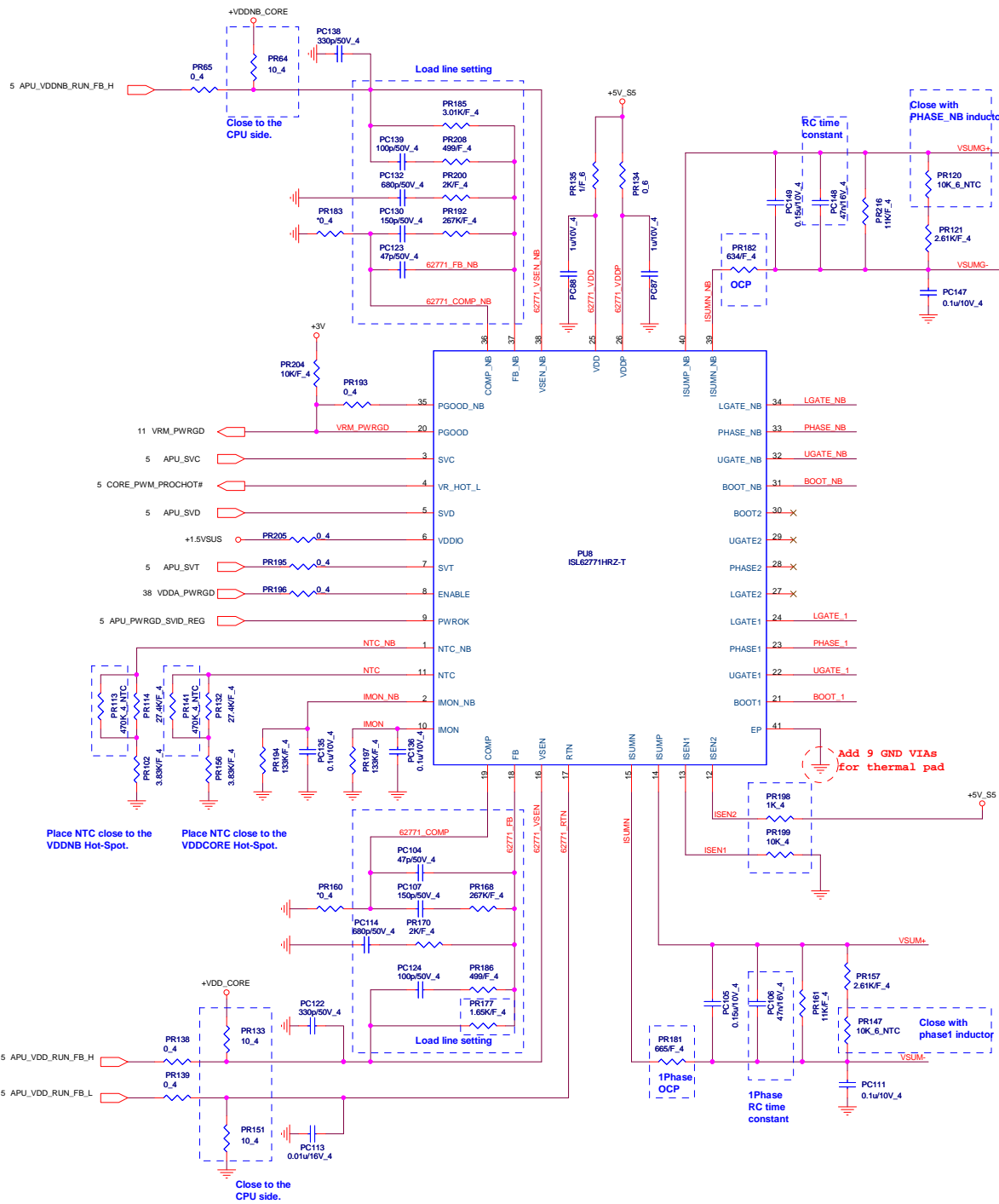
$$V_{out} = 0.8(1 + R1/R2) = 2.5V$$



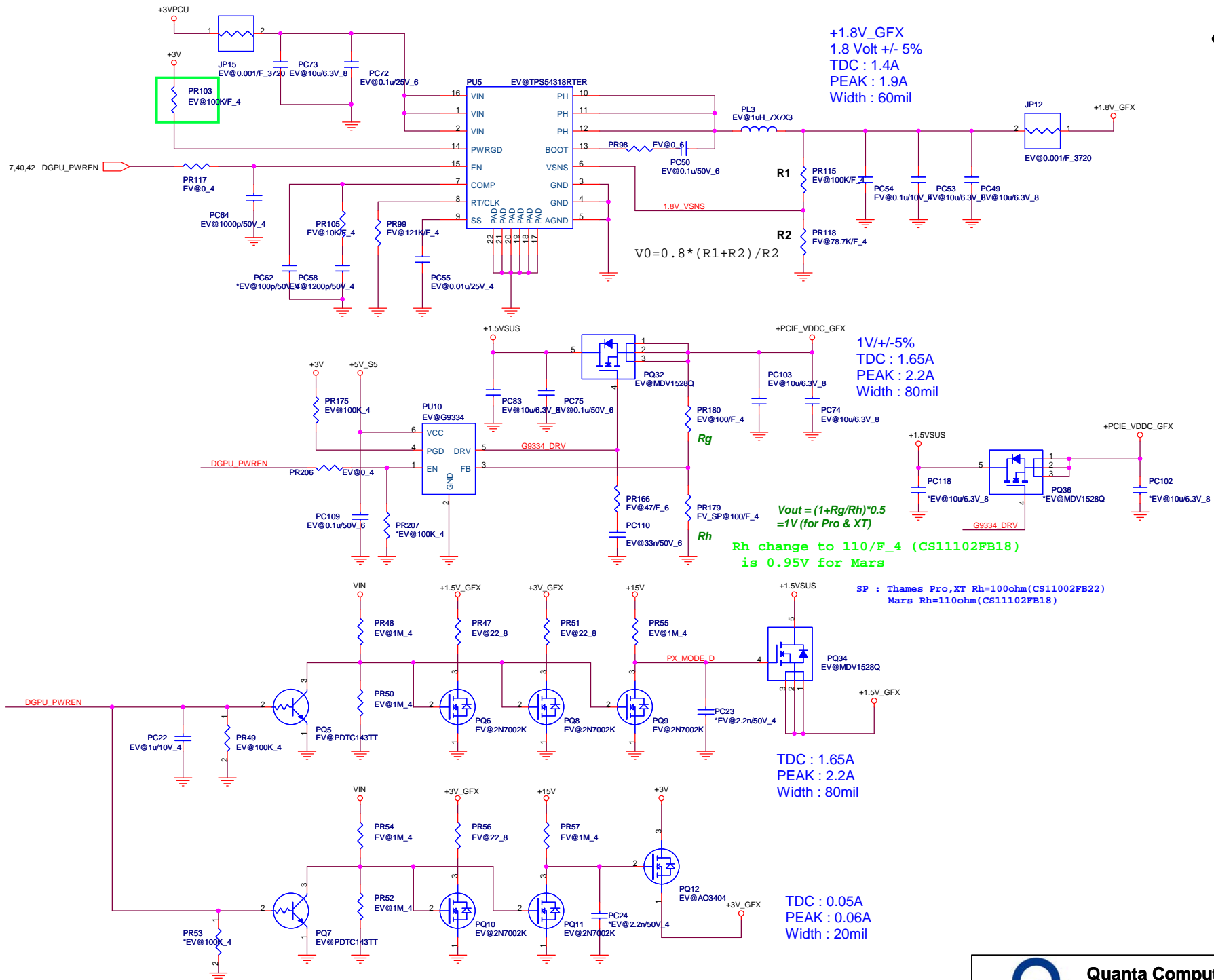
Quanta Computer Inc.

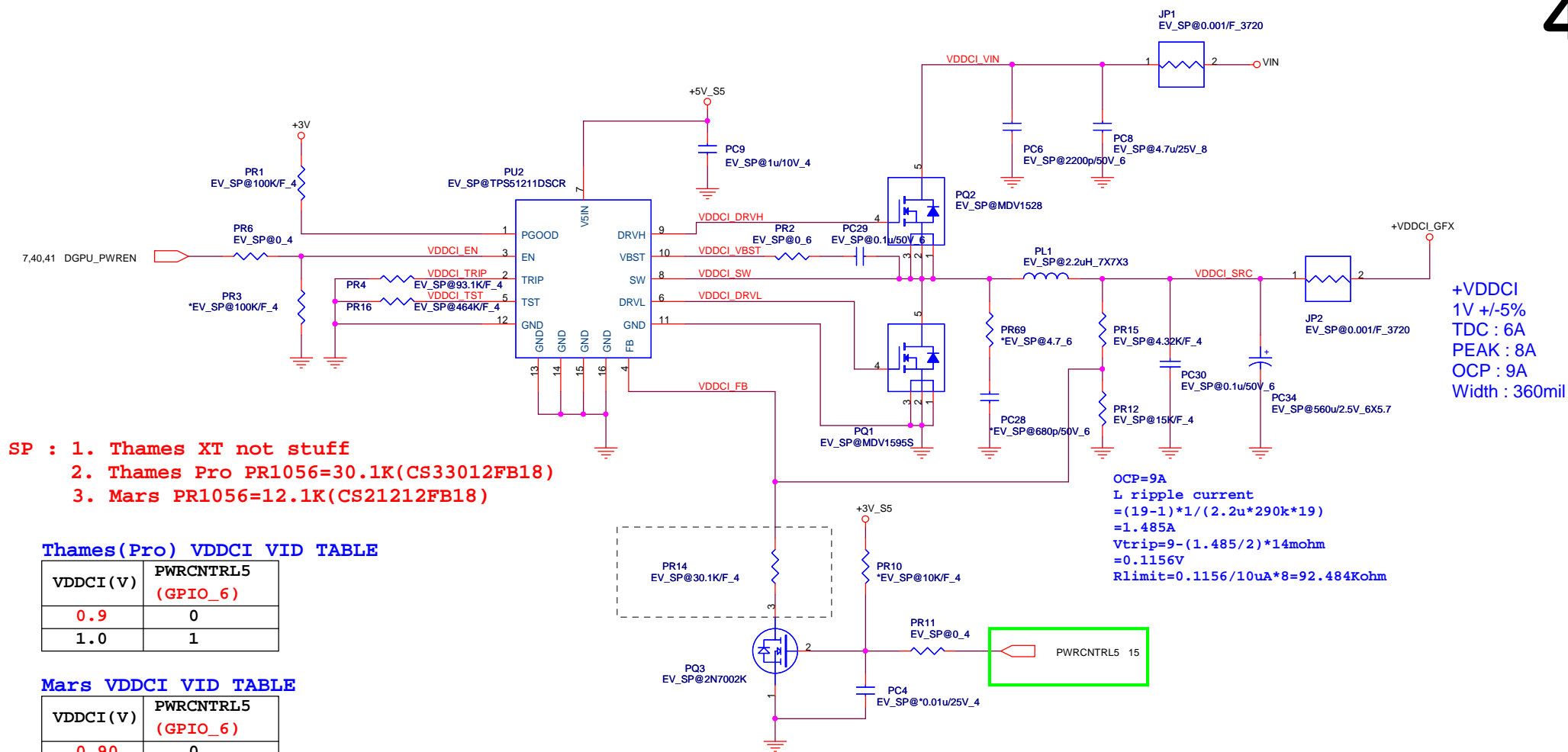
PROJECT : ZRP

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Date:	Friday, June 01, 2012	Sheet 38 of 44











MODEL		REV	CHANGE LIST			Model	ZRP MB BOARD	
						Page	From	To
ZRP M/B		A	First Release			1		
						2		
						3		
						4		
						5		
						6		
						7		
						8		
						9		
						10		
						11		
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						39		
						40		
						41		
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